A 13.1% Tuning Range 115GHz Frequency Generator Based on Injection-Locked Frequency Doubler in 65nm CMOS

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mmW and SubTHz applications

- huge bandwidth for high data rate communications
- radars and imaging: (1) security and surveillance, (2) industrial process controls, (3) medical diagnosis
- chemical sensors (spectrometers)

Effort toward cost effective CMOS solution
Outline

- Issues in LO generation at high frequency
- Conventional mmW frequency doublers
- Proposed injection-locked solution
- Test chips design
- Experimental results
- Conclusions
VCOs at fundamental frequency

State of the art 60GHz VCOs display ~10% Tuning Range

Scaling to 120GHz (assuming constant Q):

\[
\omega_{osc} = \frac{1}{\sqrt{LC}}
\]

\[
R_P = \omega_{osc} LQ
\]

\[
g_m R_p > 1
\]

- ✓ constant Q is very optimistic
- ✓ higher current and tech. scaling give marginal benefits

<table>
<thead>
<tr>
<th></th>
<th>60GHz</th>
<th>120GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td></td>
<td>L/2</td>
</tr>
<tr>
<td>C</td>
<td></td>
<td>C/2</td>
</tr>
<tr>
<td>(R_p, g_m)</td>
<td>(R_p, g_m)</td>
<td></td>
</tr>
<tr>
<td>(C_{active})</td>
<td>(C_{active})</td>
<td></td>
</tr>
<tr>
<td>(C_v)</td>
<td>~(C_v/10)</td>
<td></td>
</tr>
<tr>
<td>10% T.R.</td>
<td>2.5% T.R.</td>
<td></td>
</tr>
</tbody>
</table>
Half frequency VCO + doubler

- Tuning range preserved
- Phase noise improvement due to higher Q of passives
- Power saving in the prescaler of the PLL

Poor performances of conventional CMOS doublers
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mmW doublers: mixer

The same half-frequency signal feeds the RF and LO ports of a Gilbert mixer.

\[
\cos(\omega_0 t) \quad \xrightarrow{K_m} \quad \frac{K_m}{2}(1+\cos(2\omega_0 t))
\]

- DC offset
- High power dissipation
- Large input capacitance
- Not compatible with low supply voltage
Single ended output, conversion loss

Trade-off between conv. loss and dev. size (input cap.)
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Proposed injection-locking doubler

A push-push pair locks a differential oscillator

- Differential output
- Amplitude set by $I_{DC}$ (independent of input signal and dev. size)
- No trade off between conv. gain and input capacitance
Circuit topology

\[ \omega_0 = \frac{1}{\sqrt{\frac{L}{2} \cdot C}} \]

C-L-C and \( M_1 \) form a Pierce oscillator

\( M_2'-2'' \) inject the double frequency locking current

Supply provided by a choke inductor

\( C_{CM} \) balances the two outputs
Common-mode rejection by means of $C_{\text{CM}}$

$C_{\text{CM}}$ forms a series resonator with $L/2$ and \textit{shunts to ground} the common mode.

\[ \frac{1}{\sqrt{\frac{L}{4} C_{\text{CM}}}} = \omega_0 \]

\[ \Rightarrow C_{\text{CM}} = 2C \]
Effect of $C_{CM}$: simulations

Without $C_{CM}$:
- Amp. mismatch 6dB
- Phase mismatch 30°

With $C_{CM}$:
- Amp. mismatch < 1dB
- Phase mismatch < 5°
Circuit analysis (1/2)

\[
\begin{align*}
V_1 e^{j\varphi_1} &= -Z_T \cdot I_{osc} e^{j\varphi_1} - Z \cdot I_{inj} \\
V_2 e^{j\varphi_2} &= -Z \cdot I_{osc} e^{j\varphi_1} - Z_T \cdot I_{inj}
\end{align*}
\]

\[
\begin{pmatrix}
Z_{11} & Z_{12} \\
Z_{21} & Z_{22}
\end{pmatrix} = 
\begin{pmatrix}
Z_T \\
Z_T \\
Z
\end{pmatrix}
\]

\[
Z \approx \frac{R}{2} \frac{1}{1 + j2Q \frac{\Delta\omega}{\omega_0}}
\]

\[Z_T \approx -Z\]
Circuit analysis (2/2)

Locking range:

\[
\frac{\Delta \omega}{\omega_0} \bigg|_{\text{max}} \approx \frac{1}{2Q} \frac{I_{\text{inj}}}{I_{\text{osc}}} \sqrt{1 - \left(\frac{I_{\text{inj}}}{I_{\text{osc}}}\right)^2}
\]

- increase \( I_{\text{inj}} \) to enlarge locking range
  - increase size or bias current of the push-push pair
  - increase input swing
Locking range

[Graph showing the relationship between locking range and input amplitude. The graph includes a circuit diagram with labeled components: $V_{i+}$ and $V_{i-}$, $I_{inj}$, 10um, 65nm, 3mA, and calculated simulations marked with diamonds.]
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Two chip versions:  
(1) multiplier driven off-chip 
(2) multiplier driven by an on-chip VCO 

- \( f_{\text{out}} = 115\text{GHz} \)
- \( M_1: 20\text{m}/65\text{n}; \ M_2':-2'':10\text{m}/65\text{n} \)
- Caps. made of parasitics only
- 80\(\mu\)H single-turn resonator inductance
- loaded Q ~ 4
- \( I_1=I_2=3\text{mA} \); \( V_{\text{dd}}=1\text{V} \)
Input balun

input imp. of the push-push pair

![Circuit Diagram]

**Measured Input Matching**

![Graph]

- Frequency [GHz]
- $S_{11}$ [dB]

-40 to 65

-35 to -5

-5 to -15

-25 to -35
On-chip VCO

Single turn 100pH spiral
Fine tuning with aMOS varactor
Coarse 1bit tuning to reduce $K_{VCO}$

Device layout for minimum parasitics:

-113 dBc/Hz @ 10MHz phase-noise

C. Cao, JSSC June 06
Buffer

2-stages buffer/mixer:
• 3dB loss in the buffer configuration
• 16dB loss when 2\textsuperscript{nd} stage works as a down-converter

17mW from 1V supply
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Chip photographs

- CMOS 65nm GP from STMicroelectronics
- Active area < 200um x 200um
Experimental setups

On-chip down-conversion to V-band (50-75GHz)

Measurements at real output frequency
Single-ended output swing

Amplitude [dB]

Frequency [GHz]

direct measurements

on-chip mixing
Amplitude matching

ΔAmplitude [dB] vs Frequency [GHz]
Phase Noise

![Phase Noise Graph]

- **Phase Noise [dBc/Hz]**
- **Frequency Offset [Hz]**

- **Doubler Output**
- **Source**
VCO + doubler

Single ended power [dBm]

on-chip down-conversion

13.1 % T.R.
Phase noise of VCO + doubler

-97 @ 3MHz
-107 @ 10MHz
# Summary and comparison

<table>
<thead>
<tr>
<th>Ref.</th>
<th>$f_0$ [GHz]</th>
<th>Phase Noise [dBc/Hz @10MHz]</th>
<th>Tuning Range [%]</th>
<th>$P_{diss}$ [mW]</th>
<th>$\text{FoM}_T$ [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[3]</td>
<td>98.0</td>
<td>-102.7</td>
<td>2.55</td>
<td>7</td>
<td>-162.2</td>
</tr>
<tr>
<td>[3]</td>
<td>105.2</td>
<td>-97.5</td>
<td>0.19</td>
<td>7.2</td>
<td>-134.9</td>
</tr>
<tr>
<td>[4]</td>
<td>114.0</td>
<td>-107.6</td>
<td>2.10</td>
<td>8.4</td>
<td>-165.9</td>
</tr>
<tr>
<td>[5]</td>
<td>109.2</td>
<td>-105.2</td>
<td>2.24</td>
<td>9.6</td>
<td>-163.1</td>
</tr>
<tr>
<td>[5]</td>
<td>122.8</td>
<td>-100.2</td>
<td>1.30</td>
<td>9.6</td>
<td>-154.4</td>
</tr>
<tr>
<td>[5]</td>
<td>139.6</td>
<td>-93.0</td>
<td>0.86</td>
<td>9.6</td>
<td>-144.8</td>
</tr>
<tr>
<td>[6]</td>
<td>102.2</td>
<td>-100.9</td>
<td>4.12*</td>
<td>7.6</td>
<td>-164.6</td>
</tr>
<tr>
<td>This Work</td>
<td>115</td>
<td>-107</td>
<td>13.1</td>
<td>12</td>
<td>-179.8</td>
</tr>
</tbody>
</table>

*32nm SOI-CMOS

$$\text{FoM}_T = \text{PN}(\Delta f) - 20\log\left(\frac{f_0}{\Delta f} \times \frac{T.R.}{10}\right) + 10\log\left(\frac{P_{diss}}{1\text{mW}}\right)$$
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Conclusions

• A new circuit topology of frequency doubler, based on injection-locking has been presented.

• Compared with conventional doublers, it provides a differential output and high output swing.

• Combined with an half frequency VCO, the doubler leads to a record tuning-range beyond 100GHz and more than 10dB FoM improvement.