CMOS Integrated Circuits for Millimeter-Wave Applications

Andrea Mazzanti

Topics on Microelectronics (TOM), May 2011

Outline

- mmWave applications & CMOS technology
- Components and building blocks
- Examples from research activity in Pavia
mm-Wave applications

- Gbit/s Wireless connectivity: 60GHz
- Automotive radars: 22-29GHz, 77-81GHz
- mmWave camera (Imaging systems): 35GHz, 94GHz, 140GHz, 220GHz
- mmWave nose (chemical sensors): 200 – 300GHz

Gbit/s wireless connectivity at 60GHz

- 7 GHz of unlicensed bandwidth
- Potentially more than 10Gbit/s wireless connectivity
- High O2 attenuation -> improve security & spectrum reuse
Gbit/s wireless connectivity at 60GHz

Leveraging the availability of wide spectrum for high rate transfer

W-LAN / MAN

W-PAN

Point to Point Link
100m - 1km
1.8Gbps - 1Gbps

High speed wireless LAN
100 Mbps ~ 1Gbps

Wireless home video
and data link

IEEE 802.15.3 mmWIG

Standardizations of Gbit/s connectivity

- Many standardization activities by the Industry
- Interoperability and coexistence taken into account
- Single carrier (low distance / low rate) and OFDM (high rate, high distance)
- Channels bonding for high rate transfer

<table>
<thead>
<tr>
<th>Forum</th>
<th>Status</th>
<th>Max. data rate</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECMA-387</td>
<td>2nd version released: Dec 2010</td>
<td>6.35 Gbit/s per channel, 25.4 Gbit/s (4 channels max.)</td>
<td>High-data-rate WPAN transport for both bulk data transfer and multimedia streaming</td>
</tr>
<tr>
<td>IEEE 802.15.3c</td>
<td>Released: Oct. 2009</td>
<td>5.8 Gbit/s</td>
<td>High-data-rate WPAN specification</td>
</tr>
<tr>
<td>IEEE 802.11ad</td>
<td>PAR approved, release: Dec 2012</td>
<td>&gt; 6.8 Gbit/s</td>
<td>WLAN in the 60 GHz band</td>
</tr>
<tr>
<td>Wireless Gigabit Alliance (WiGig)</td>
<td>Common standardization with IEEE 802.11ad</td>
<td></td>
<td>Global wireless ecosystem of interoperable, high-performance devices (CE, PC, IC, handheld)</td>
</tr>
</tbody>
</table>
Automotive Radars

- 22-29 GHz & 77-81GHz
- Short-range radar: parking assist, object detection
- Long-range radar: automatic cruise control, low visibility (fog), object detection
- Long range vision: automatic driver

Radar Operating Principle

<table>
<thead>
<tr>
<th>Depth Resolution</th>
<th>$\Delta_z = \frac{ct}{2\sqrt{\varepsilon_r}} - \frac{c}{2(BW)\sqrt{\varepsilon_r}}$</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lateral Resolution</td>
<td>$\Delta_{x,y} = \frac{R\lambda}{D}$</td>
<td>Frequency</td>
</tr>
<tr>
<td>SNR</td>
<td>$P_r = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 R^4}$</td>
<td>TX power</td>
</tr>
</tbody>
</table>
Radar Specifications

A Single-Chip Dual-Band 22–29-GHz/77–81-GHz BiCMOS Transceiver for Automotive Radars

Vipul Jain, Student Member, IEEE, Fred Tseng, Student Member, IEEE, Lei Zhou, Student Member, IEEE; andParviz Heidari, Senior Member, IEEE

TABLE I
RADAR SYSTEM-LEVEL SPECIFICATIONS

<table>
<thead>
<tr>
<th>Frequency Range</th>
<th>22-29 GHz</th>
<th>77-81 GHz(a)</th>
<th>77-81 GHz(b)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmit peak EIRP</td>
<td>21.5 dBm</td>
<td>55 dBm</td>
<td>26.1 dBm</td>
</tr>
<tr>
<td>Receiver Antenna Gain</td>
<td>15.6 dBi</td>
<td>15.6 dBi</td>
<td>15.6 dBi</td>
</tr>
<tr>
<td>Signal Bandwidth</td>
<td>7 GHz</td>
<td>4 GHz</td>
<td>4 GHz</td>
</tr>
<tr>
<td>RX Noise Figure(a)</td>
<td>4.5 dB</td>
<td>8 dB</td>
<td>8 dB</td>
</tr>
<tr>
<td>Required SNR</td>
<td>11 dB</td>
<td>11 dB</td>
<td>11 dB</td>
</tr>
<tr>
<td>Single-pulse SNR</td>
<td>1.1 dB</td>
<td>24.9 dB</td>
<td>-1.2 dB</td>
</tr>
<tr>
<td>Number of integrated pulses</td>
<td>10</td>
<td>1</td>
<td>17</td>
</tr>
</tbody>
</table>

\(a\)Assuming maximum allowable EIRP by ETSI.
\(b\)Assuming maximum EIRP based on measured results from our transmitter (=10.5+15.6).
\(c\)Based on receiver measurements.

mmWave Imaging

Source: M.Sato & K.Mizuno, “mmWave Imaging Sensor”

- Objects emit and reflect mmWave radiation
- mmWaves are much more effective (lower attenuation) than infrared in poor weather conditions, clouds, fog, snow, rain, dust, clothes
- Envisioned applications include: security and surveillance, driving assistance, medical imaging, industrial process and quality control
- 34GHz, 94GHz, 140GHz, 220GHz
mmWave Imaging

Passive (radiometer)

Measure the radiated power: $T_{obj} = \varepsilon T_a$

Very weak received signals (basically thermal noise). Low noise, high sensitivity RX very important

mm-Wave source (illuminator) not required

Comply with Radio Emissions Law regulations

Active

Measure the reflected power: $T_{obj} = \rho T_{source}$

Larger SNR. Tolerate better RX noise

Expensive, high power, mm-Wave source (illuminator) is required

mmWave Imaging

Image contrast set by the minimum detectable temperature difference ($\Delta T_{min}$)

$\Delta T_{min}$ is determined by detector noise and integration time

Source: M.Sato & K.Mizuno, “mmWave Imaging Sensor”

Heterodyne detector:
low noise, high power, high cost

Preamplified direct detector

Direct detector:
poor noise, low power, lower cost
Passive mmWave (PMMW) Image example from “M.Sato & K.Mizuno, “mmWave Imaging Sensor”

94GHz operation frequency. Preamplified detector, InP HEMT technology. Temperature resolution 1K, with 10msec integration time. 2.5m distance from the target Image constructed by mechanical repositioning a 10 x 4 receivers array

Active mmWave Image example from “A.Tang & M.-C. F. Chang, IEEE ISSCC 2011”

The pixel is a regenerative receiver. 65nm CMOS, 13.5mW x pixel.

180GHz operating frequency
Like a radio: transmits through a chamber and measures the received signal strength
Repeat varying frequencies to determine frequency response.
Identify contents of the sample

Electronic nose:
monitoring toxic gas,
pollution, air quality,
xplosives, illicit drugs.

- Carbon Monoxide, CO ( >50 ppm un-safe, 230.538 GHz)
- Formaldehyde, CH₂O (>100 ppb un-safe, 211.211 GHz)
- Hydrogen Cyanide, HCN (>15-50 ppm/h un-safe, 265.889 GHz)
- Phosphine, PH₃ (>0.3ppm un-safe, 266.945 GHz)
- Ethanol (CH₃CH₂OH, 40 ppm legal limit), Methanol and Acetone (many lines between 180-300 GHz)
CMOS Technology

Opportunity and challenges

Why CMOS technology

- Speed of MOS transistors is continuously improving with scaling
- Cheaper, for large volumes, compared to SiGe BiCMOS and III-V technologies
- Unprecedented integration level with power digital signal processing (DSP), analog circuits and antennas
- Passive devices (transmission lines, inductors, capacitors) easier to integrate (less area) at higher frequencies
- Communication and computing applications have benefited from these trends
- First mmWave CMOS circuits from Berkely at ISSCC 2004, CMOS 0.13um, 60GHz frequency
**Cut-off Frequency**

![Graph showing cut-off frequency over years, with CMOS overtaking SiGe in 2009 and InP in 2014.]

**Supply Voltage & Output Conductance**

- in 65nm node ($f_T \sim 160$GHz) $g_m/g_{ds} \sim 6$, $V_{dd}=1V$
- $g_m/g_{ds}$ represents maximum voltage gain
- Low supply voltage limits dynamic range and linearity of amplifiers, output power and efficiency of PAs, phase noise of oscillators
- Issues common to Analog design but at mmWave:
  - must use $L_{min}$ and high current density for speed ($f_T$)
  - cascodes introduce parasitic poles
  - Current-mode circuit techniques not yet applicable

J.Pekarik et al., IEEE CICC 2004
Losses of parasitic capacitors

- Large polysilicon gate resistance ($r_g$) at small gate length
- $r_g$ is responsible for power dissipation when AC current flows through $C_{gs}$

$$Q_g = \frac{\text{Energy stored in } C_{gs}}{\text{Energy dissipated on } r_g} = \frac{1}{2\pi f \cdot C_{gs} \cdot r_g}$$

Example: 20x1um / 65nm nMOS device has $r_g \sim 16\Omega$, $C_{gs} \sim 28fF$

$$Q_g @ 60GHz = 5.9 \quad Q_g @ 6GHz = 59$$

Passive Components

Back-End Of Line (BEOL) scaling critical for passive components:

- Shrinking of the metal layers leads to:
  - Larger metals resistance ($R_s$, losses)
  - Larger substrate parasitics ($C_{sub}$, $R_{sub}$)
RF vs mmWave CMOS design

First CMOS RF products (5GHz) with 250nm tech. node
First CMOS mm-Wave products (60GHz) with 90nm tech. node

<table>
<thead>
<tr>
<th>fo</th>
<th>5 GHz</th>
<th>60 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>250 nm</td>
<td>90 nm</td>
</tr>
<tr>
<td>$f_T$</td>
<td>20 GHz ($4 \times fo$)</td>
<td>120 GHz ($2 \times fo$)</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.5V</td>
<td>1.2V</td>
</tr>
<tr>
<td>$gm/gds$</td>
<td>15.2</td>
<td>10.6</td>
</tr>
<tr>
<td>Q of gate capacitance</td>
<td>&gt; 40</td>
<td>~6</td>
</tr>
<tr>
<td>Inductor Q</td>
<td>10-15</td>
<td>15-20</td>
</tr>
</tbody>
</table>

Outline

- mmWave applications & CMOS technology
- *Devices and building blocks*
- Examples from research activity in Pavia
Device Modeling

CMOS technology Design Kits (DKs) usually do not support mm-Wave design:
- device models are not very accurate beyond 10 – 20 GHz
- mmWave components not characterized or missing (e.g. very small inductors and capacitors, TLINEs)

Device customizations, optimizations, measurement and modeling is a key step for mmWave design

Active Devices

- Layout of transistors determines extrinsic parasitics and strongly affect performances

\[ f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} \]

\[ f_{max} \approx \frac{f_T}{2\sqrt{R_g(g_{ds} + f_TC_{gd})}} \]

- Maximum frequency of oscillations, \( f_{max} \) is a good figure of merit:
  - minimize \( R_g \)
  - minimize \( C_{gd} \)
  - maximize \( f_T \)
Minimize Rg & Cgd

- Larger spacing between gate (G) and drain (D) contacts may help to reduce Cgd

Top view  Side view  Top view  Side view

- Gate resistance: double gate contacts and many small fingers in parallel

\[ R_{g}' = \frac{R_g}{16} \]

\[ R_G \approx \frac{1}{12} \cdot R_{\text{poly}} \cdot \frac{W}{L} \cdot \frac{1}{n_f^2} \]

\[ f_{\text{max}} \]

For given device size and layout, \( f_T \) is maximized by maximizing \( g_m \)

\[ f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} \]

\[ f_{\text{max}} \approx \frac{f_T}{2\sqrt{R_g(g_{ds} + f_T C_{gd})}} \]
Active Device Modeling

Suzuki et al. IEEE ISSCC-08

Compact MOS model provided in design-kit

MOS compact models supplied with Design Kit do not support mm-Wave operation
CAD tools for parasitic extractions not enough accurate to model interconnect parasitics

Accurate MOS models add parasitics (from measurements and/or electromagnetic simulations) around the device compact model (e.g. BSIM)

Inductors & Capacitors Modeling

- frequency dependence of losses (skin effect)
- differential vs single-ended excitations
- substrate losses

- [Graphs showing frequency dependence of inductance and capacitance]
Transmission Lines

- short $\lambda$ at mmWaves makes TLINES small enough to be used on-chip
- long interconnections between building blocks
- confinement of EM fields minimize cross-talk and spurious coupling between blocks
- emulate lumped components (capacitors, inductors)
- matching networks, phase shifters

TLINEs are inherently scalable in length and are fully characterized by:

- characteristic impedance: $Z_0$
- attenuation constant: $\alpha$
- phase constant: $\beta$

Usually not available in standard CMOS Design Kits

Compact models for circuits design made of several RLC networks

F. Vecchi et al.: IEEE JSSC 2009
CMOS Building Blocks:

- **Low Noise Amplifiers (LNAs)**
- Mixers
- Voltage Controlled Oscillators (VCOs)
- Power Amplifiers (PAs)

**Low Noise Amplifier**

- LNA must provide low NF and high gain
- 50 ohm input impedance
- Unconditional stability against variations of the antenna impedance
- Linearity requirements less critical than for RF applications

\[ F_{RX} = F_{LNA} + \frac{F_{rest} - 1}{G_{LNA}} \]
Common Gate (CG) LNA

- L1 resonates at input, improving matching.
- L2 resonates at output.
- Relatively stable
- NF 4-5 dB
- Broadband input matching
  \[ R_{in} = \frac{R_1 + r_o}{1 + (g_m + g_{mb})r_o} \]
- Limited Gain
  \[ \frac{V_{out}}{V_{in}} \approx 1.75 \] (4.8dB)

Common Source (CS) LNA

- L1 resonates at output
- Stability concerns due to Cgd
- Relatively high gain, thanks to contribution of the matching network
  \[ \frac{V_{out}}{V_{in}} = \frac{1}{2} \sqrt{\frac{r_g \cdot Q^2_{gd}}{50}} \cdot g_m \cdot R_L \]
- Gain 9-12 dB
- NF ~ 5.5-6.6 dB

Matching on a noisy resistance (r_g) introduces a 3dB lower bound on NF

Ex: \( r_g = 16\Omega, Q_g = 6 \) at 60GHz
\[ \rightarrow A_{\text{match}} = 4.6dB \]
Inductively Degenerated (ID) CS - LNA

- Ls introduces a noiseless real part on the input impedance at the gate:
  \[
  Z_i = (r_g + \omega T L_s) + j \left( \omega L_s - \frac{1}{\omega C_{gs}} \right)
  \]

- Eliminates the 3dB lower bound on NF but loses gain from the matching network
- More noise contribution from load and following stages
- Lower gain from matching network

\[
\begin{align*}
\frac{V_{gs}}{V_{in}} &= \frac{i_g}{r_g} \cdot (r_g + \omega T L_s) \\
V_{gs} &= \frac{i_g}{j\omega_0 C_{gs}}
\end{align*}
\]

Ex: 3dB penalty if \( \omega T L_s = r_g \)

Cascode LNA

- Improve stability and gain of CS & ID-CS LNAs
- Performance penalty due to \( C_x = C_j + C_{gs2} \)
- Additional L resonating with \( C_x \)
- \( \Pi \) matching network with L and parasitics
- Gain boost
LNA Example - I

[Heydari et al, JSSC 2007]

- 90nm CMOS, center frequency 63GHz, 3dB bandwidth 4.5GHz
- Gain 12.2dB, Isolation $S_{12} < -8$dB
- Noise Figure 6.5 dB
- Power dissipation 10.5 mW

LNA Example - II

[T. Yao et al, JSSC 2007]

- 90nm CMOS, center frequency 58 GHz, 3dB bandwidth 8GHz
- Gain 14.6dB, Isolation $S_{12} < -30$dB
- NF < 5.5 dB (estimated from indirect measurements)
- Power dissipation 24 mW from 1.5V
LNA Example - III

[Weyers et al, ISSCC 2008]

- 65nm CMOS, center frequency 60GHz, 3dB bandwidth 7.7GHz
- Gain 22.3dB, Isolation S12 < -40dB
- NF 6.1 – 6.7 dB
- Power dissipation 35 mW from 1.2V

CMOS Building Blocks:
- Low Noise Amplifiers (LNAs)
- Mixers
- Voltage Controlled Oscillators (VCOs)
- Power Amplifiers (PAs)
Mixers

- Mixers translate spectrum of the signal: \( \omega_{in} - \omega_{LO} \) in RX, \( \omega_{in} + \omega_{LO} \) in TX
- Need non-linearity or time-variance
- For RX, low noise and good conversion gain
- High LO to IN and LO to IF isolation required
- High input impedance (LO and IN ports) desirable

Single Gate Mixers

- Exploit 2nd order non-linearity of the device

\[
i_D \propto \beta \cdot (V_{in} \cos(\omega_{in} t) + V_{LO} \cos(\omega_{LO} t))^2
\]

\[
i_D \propto \beta \cdot V_{in} V_{LO} \cos[(\omega_{in} - \omega_{LO}) t] + other harm. comp.
\]

- Selective load rejects undesired harmonic components
- Conversion Loss and Noise
- Low \((V_{gs} - V_{th})\) and large LO required
- Poor LO to IN isolation, LO feed-through
Switching Mixers

- Exploit time variance: multiply signal by the sign of LO
  \[ V_{IF} = \begin{cases} +v_{in}gm_1Z_L & \text{if } V_{LO} > 0 \\ -v_{in}gm_1Z_L & \text{if } V_{LO} < 0 \end{cases} \]

- Large conv. gain and low noise
- Lends to differential IF (need diff. LO)
- Good LO to IN isolation
- Simple modification to fully balanced (Gilbert Cell) to eliminate LO feedthrough

Switching Mixers

- Low LO amplitude, low gain of M2', M2'' and pole at P (< f_T/2 ) limit gain and noise performances

- \( L_5 \) resonates with cap at node P.
- Lower current through M4-M5 allows more abrupt switching.
- Simulations, CMOS 90nm:
  10.2dB gain, 12.5dB NF, ~ 17mW

[Razavi, VLSI Symp.97], [Razavi JSSC 2008]
CMOS Mixer Example - I

[Doan et al, RFIC Symp.05]

- Balanced Single Gate Mixer, 0.13-um CMOS at 60 GHz
- LO power 0dBm
- Conversion loss = 2 dB
- NF = 13.8 dB
- Power consumption = 2.4 mW

CMOS Mixer Example - II

[Afshar et al, ISSCC 2008]

- Switching Mixer, 90nm CMOS at 60 GHz
- LO with a on-chip transformer. Required LO power -2.5dBm
- Mixer simulations: 6.5dB conv. gain with 6.5mW power
- LNA + Mixer: 18dB gain, 6.1dB NF
CMOS Mixer Example - III

Khanpour et al, JSSC 2008

- Fully balanced switching Mixer, 65nm CMOS 74GHz – 91GHz
- Conv. Gain 4dB, NF 8-10dB, LO power 5dBm
- 13mW from 1.5V

CMOS Building Blocks:
- Low Noise Amplifiers (LNAs)
- Mixers
- Voltage Controlled Oscillators (VCOs)
- Power Amplifiers (PAs)
Voltage Controlled Oscillator (VCO)

- Main block of the synthesizer, provides LO for mixers
- Oscillator with output frequency set by $V_{ctrl}$
- Large output signal swing desirable
- Frequency tuning enough to cover channels + processing spreads
- High spectral purity (low phase noise)

MOS Varactor

Trade-off between Quality Factor ($Q_v$) and capacitance variation $C_{\text{max}}/C_{\text{min}}$

Measurements at 24GHz

For $L_g=200\text{nm}$

$$\frac{C_{\text{MAX}}}{C_{\text{MIN}}} = 3 \quad \frac{\Delta C}{c} = 100\%$$

At 60GHz $Q_v \sim 2.5$ times lower than 24GHz

$Q_v @ 24\text{GHz} = 15$

$Q_v @ 60\text{GHz} = 6$
LC-Tank VCO

At LC resonance:

\[ \omega_{osc} = \frac{1}{\sqrt{LC}} \quad g_{m1,2}R_p > 1 \]

\( R_p \) represents tank losses

A comparison with RF:

60 GHz: \( Q_L=15, Q_C = 6 \) → \( Q_T = 4.2 \) Varactors limit \( Q_T \)

5 GHz: \( Q_L=10, Q_C > 40 \) → \( Q_T > 8 \) Inductors limit \( Q_T \)

Two times more losses → ~ two times more \( g_m \) for oscillator start-up
**Tuning Range**

\[ T. R. = \frac{\Delta f}{f_0} \approx \frac{1}{2} \frac{\Delta C}{C} \]

- Assuming only the varactors, \((\Delta C/C_V = 100\%)\):
  \[ T. R. = \frac{\Delta f}{f_0} \approx \frac{1}{2} \frac{\Delta C}{C_V} = 50\% \]

- Unfortunately the tank is loaded by many fixed capacitive contributions (parasitics, load)

- \(C_V\) hardly exceed 30\% of the total tank capacitance \((C_{tank})\)

\[ T. R. = \frac{\Delta f}{f_0} \approx \frac{1}{2} \frac{\Delta C}{C_V} \cdot \frac{C_V}{C_{tank}} = 15\% \]

**Phase Noise**

Noise of the devices perturbs randomly the zero crossing of the oscillator output signal

\[ L(\Delta f) \propto 10 \cdot \log \left( \frac{P_{noise \ in \ 1Hz \ bandwidth @ \Delta f}}{P_{signal}} \right) \]
**Phase Noise**

\[
L(\Delta f) \propto \frac{k_B T R_P}{V_{osc}^2} \cdot \frac{1}{Q_T^2} \cdot \left(\frac{f_{osc}}{\Delta f}\right)^2
\]

- Maximize \( Q_T \) → trade-off with T.R.
- Maximize \( V_{osc}^2 / R_p \):

\[
\begin{align*}
V_{osc} & \sim R_P I_B \\
V_{osc\_max} & \sim V_{dd} \\
\frac{V_{osc\_max}^2}{R_P} & \sim I_B V_{dd}
\end{align*}
\]

Power Dissipation

A comparison with RF:

- 60 GHz, \( Q_T = 4.2 \)
- 5 GHz, \( Q_T > 8 \)

\[
\left(\frac{60\text{GHz}}{5\text{GHz}}\right)^2 \left(\frac{8}{4.2}\right)^2 = 522
\]

60GHz VCO would require 522 x power dissipation for the same phase noise...

---

**VCO example - I**

[Bozcola et al, RFIC 2008]

- 65nm CMOS, 7.2mW from 1.2V supply
- Analog + Digital Switching of Varactors
- 51GHz to 57.2GHz frequency, T.R. 11.5%
- Phase Noise @ 10MHz offset -118dBc/Hz
VCO example - II

[Cao et al, Electronics Letters, 2006]

- Push-Push VCO: extract 2nd harm. of $f_{osc}$ from a common-mode node
- 0.13μm CMOS, 16.5mW from 1.5V
- 191.4 GHz to 192.7 GHz frequency, T.R. 0.68%
- Phase Noise @ 10MHz offset -106dBc/Hz

CMOS Building Blocks:
- Low Noise Amplifiers (LNAs)
- Mixers
- Voltage Controlled Oscillators (VCOs)
- Power Amplifiers (PAs)
Power Amplifier

- Deliver mmWave power to the antenna
- Stability against load impedance variation
- Linearity very important (efficient modulation needs linear amplification)
- Power efficiency
- Power gain: multiple stages (PA + driver(s))
- Device stress: long time reliability

Class-A for max power gain and linearity. $L_1$ resonates with cap. at node X

$V_{max}$ (0-pk drain swing) $V_{DD}$

Given the power ($P$) and $V_{max}$, $R_{in}$ is calculated from

$$P = \frac{V_{max}^2}{2R_{in}}$$

Drain voltage $> V_{DD}$: long term reliability concerns

for a RF voltage $> 60\%$ of nominal supply, $P_{out}$ degrades by 2dB over 7 years

[Ruberto, IEEE RFIC 2005]
Power Efficiency

Finite Q of passive components, low supply voltage and Class-A operation limit drastically the power efficiency.

Numerical Example

Assume: $V_{DD}=1V$, $P_X = 25mW$, $V_{max}=0.6V$ \hspace{0.5cm} ( $V_{drain\_max}=1.6V$ )

Required $R_{in}$ is 7.2$\Omega$, $I_{in} = V_{max}/R_{in} = 83mA$ \hspace{0.5cm} (= $I_{DC}$, Class A)

$P_{diss} = V_{DD} \times I_{DC} = 83 mW$

$\eta_M1 = 30\%$
Matching Losses

Q of passives (L,C, TLINEs) responsible for matching losses

\[ \eta_{\text{match}} = \frac{1}{1 + \frac{\alpha}{Q}} \]
\[ \alpha = \sqrt{\frac{50}{R_{\text{in}}} - 1} \]

\( R_{\text{in}} \) is 7.2\( \Omega \), \( Q=5 \):
\[ \eta_{\text{match}} = 66\%, \ P_{\text{out}}=16.5\text{mW} \]
\[ \eta = \eta_{M1} \times \eta_{\text{match}} = 19\% \]

Driver Stage

- M1 very large, \( W \sim 100\text{um} \)
- Layout parasitics limit Max Gain \(- 5 - 6 \text{ dB} \)
- Output of M1 is not conjugate matched: \( G_{PM1} \sim 2-3\text{dB} \)
- Driver stage required to achieve good power gain
Driver Stage

Numerical Example Continued:

- M2 in Class A
- Assuming $\eta_{M2} \sim \eta_{M1}$ (30%), $P_{DCM2} = 40\text{mW}$

$$\eta = \frac{16.5\text{mW}}{40\text{mW} + 83\text{mW}} \approx 13.4\%$$

Power Combining Techniques

Efficiency degrades as output power increases

Use many low power PAs in parallel
- Lumped elements power combining (transformers)
- Distributed elements power combining (TLINEs)
- Spatial Power Combining (Antennas)
PA example - I

[Heydari et al, CICC 2007]

- 90 nm CMOS, 1.2V supply, 56 GHz
- Gain 9.8dB
- $P_{\text{out}_{1\text{dB}}} = 6.7 \text{dBm} \ (\sim 5\text{mW})$
- Efficiency 20%

PA example - II

[Lai & Garcia, ISSCC2010]

- 4-way transformer power combining
- 65 nm CMOS, 1.0V supply, 60 GHz
- Gain 19.2dB
- $P_{\text{out}_{1\text{dB}}} = 15.2 \text{dBm} \ (\sim 33\text{mW})$
- Peak Efficiency 11%
PA example - III

[Law & Pham, ISSCC2010]

- 4-way distributed power combining
- 90 nm CMOS, 1.2V supply, 60 GHz
- Gain 20.6dB
- $P_{out\_1dB} = 18.2\,\text{dBm} \, (\sim 65\text{mW})$
- Peak Efficiency 14.2%

Outline

- mmWave applications & CMOS technology
- Devices and building blocks
- Examples from research activity in Pavia
A 13.1% Tuning Range 115GHz Frequency Generator Based on Injection-Locked Frequency Doubler in 65nm CMOS

Enrico Monaco, Massimo Pozzoni, Francesco Svelto, Andrea Mazzanti


VCOs at fundamental frequency

State of the art 60GHz VCOs display ~10% Tuning Range

Scaling to 120GHz (assuming constant Q):

\[
\omega_{osc} = \frac{1}{\sqrt{LC}}
\]

\[
R_p = \omega_{osc} LQ
\]

\[
g_m R_p > 1
\]

\begin{array}{|c|c|}
\hline
\text{60GHz} & \text{120GHz} \\
\hline
L & L/2 \\
C & C/2 \\
R_p, g_m & R_p, g_m \\
C_{active} & C_{active} \\
C_v & \sim C_v/10 \\
10\% \ T.R. & 2.5\% \ T.R. \\
\hline
\end{array}

✓ constant Q is very optimistic
✓ higher current and tech. scaling give marginal benefits
Half frequency VCO + doubler

- Tuning range preserved
- Phase noise improvement due to higher Q of passives
- Power saving in the divider of the PLL

Frequency doubler performance is key

Doubler circuit topology

\[ \omega_0 = \frac{1}{\sqrt{L/2 \cdot C}} \]

C-L-C and M₁ form a Pierce oscillator

M₂⁻²'' inject the double frequency locking current

Supply provided by a choke inductor

C_CM balances the two outputs
Common-mode rejection by means of $C_{CM}$

$C_{CM}$ forms a series resonator with $L/2$ and shunts to ground the common mode.

$$\frac{1}{\sqrt{\frac{L}{4} C_{CM}}} = \omega_0$$

$\Rightarrow C_{CM} = 2C$

Test chips

Two chip versions:
1. Doubler driven off-chip
2. Doubler driven by an on-chip VCO

CMOS 65nm GP from STMicroelectronics
### Comparison with fundamental freq. VCOs

<table>
<thead>
<tr>
<th>Ref.</th>
<th>$f_0$ [GHz]</th>
<th>Phase Noise [dBc/Hz @10MHz]</th>
<th>Tuning Range [%]</th>
<th>Pdiss [mW]</th>
<th>FoM$_T$ [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[3]</td>
<td>98.0</td>
<td>-102.7</td>
<td>2.55</td>
<td>7</td>
<td>-162.2</td>
</tr>
<tr>
<td>[3]</td>
<td>105.2</td>
<td>-97.5</td>
<td>0.19</td>
<td>7.2</td>
<td>-134.9</td>
</tr>
<tr>
<td>[4]</td>
<td>114.0</td>
<td>-107.6</td>
<td>2.10</td>
<td>8.4</td>
<td>-165.9</td>
</tr>
<tr>
<td>[5]</td>
<td>109.2</td>
<td>-105.2</td>
<td>2.24</td>
<td>9.6</td>
<td>-163.1</td>
</tr>
<tr>
<td>[5]</td>
<td>122.8</td>
<td>-100.2</td>
<td>1.30</td>
<td>9.6</td>
<td>-154.4</td>
</tr>
<tr>
<td>[5]</td>
<td>139.6</td>
<td>-93.0</td>
<td>0.86</td>
<td>9.6</td>
<td>-144.4</td>
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<tr>
<td>[6]*</td>
<td>102.2</td>
<td>-100.9</td>
<td>4.12</td>
<td>7.6</td>
<td>-164.8</td>
</tr>
<tr>
<td>This Work</td>
<td>115</td>
<td>-107</td>
<td>13.1</td>
<td>12</td>
<td>-179.8</td>
</tr>
</tbody>
</table>

*32nm SOI-CMOS

 FoM$_T$ = $PN(\Delta f) - 20\log\left(\frac{f_0}{\Delta f} \times \frac{T.R.}{10}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right)$

---

**A Wideband mm-Wave CMOS Receiver for Gb/s Communications Employing Interstage Coupled Resonators**

Federico Vecchi, Stefano Bozzola, Massimo Pozzoni, Davide Guermandi, Enrico Temporiti, Matteo Repossi, Marco Cusmai, Ugo Decanis, Andrea Mazzanti, Francesco Svelto

"A Wideband mm-Wave CMOS Receiver for Gb/s Communications Employing Interstage Coupled Resonators" **ISSCC 2010**

High Rate 60 GHz Phy Proposal

- Large RF bandwidth (~ 9 GHz minimum)
- Minimum Sensitivity: from -60 dBm (1 Gb/s) to -50 dBm (4 Gb/s)
- Maximum Noise Figure < 10 dB
- Large LO tuning range required
- Very stringent phase noise at maximum data rate

Phase Noise Requirements

IEEE 802.15-06-0477-01-003c [Online].

- Phase noise rotates signal constellation and impairs BER
- A LO phase noise < -113dBC/Hz @10MHz offset is required in the most stringent case
Sliding IF Receiver Architecture

- First down-conversion to 1/3 of the received frequency → lower tuning-range required, relatively low power
- Only one PLL needed
- Injection Locked Dividers to generate I/Q half frequency signals

Wide-band LNA based on coupled resonators

- Gain-bandwidth trade-off in singly-tuned inter-stage loads leads to large dissipation.
- Coupled resonators are introduced to increase bandwidth and limit dissipation.
Wideband RF Mixer

Magnetic instead of capacitive coupling
Inductor required for capacitive coupling > 1nH @ 20 GHz

VCO & mmWave Dividers

Fine tuning: NMOS in NWELL varactors
Coarse tuning: switched MOM cap.
12.6 % tuning range
Area: 2.4 mm²

Power Consumption: 75 mW from 1 V

Technology: STMicroelectronics 65nm CMOS Bulk

Gain & Noise Figure Measurements

Peak gain: 35 dB over a ~13 GHz bandwidth
Noise Figure lower than 6.5 dB, with a minimum of 5.6 dB
VCO tuning range: 12.6%
Performance Summary

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Gain (High Gain)</td>
<td>35.5</td>
<td>[dB]</td>
</tr>
<tr>
<td>Voltage Gain (Low Gain)</td>
<td>14</td>
<td>[dB]</td>
</tr>
<tr>
<td>Noise Figure (High Gain)</td>
<td>5.6 – 6.5</td>
<td>[dB]</td>
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<tr>
<td>Noise Figure (Low Gain)</td>
<td>12</td>
<td>[dB]</td>
</tr>
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<td>RF Bandwidth</td>
<td>&gt;13</td>
<td>[GHz]</td>
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<tr>
<td>Image Rejection</td>
<td>80</td>
<td>[dB]</td>
</tr>
<tr>
<td>Tuning Range</td>
<td>12.6</td>
<td>[%]</td>
</tr>
<tr>
<td>I/Q Mismatch</td>
<td>&lt; 3</td>
<td>[deg]</td>
</tr>
<tr>
<td>LO Phase Noise (from 60GHz)</td>
<td>-115</td>
<td>[dBc/Hz]</td>
</tr>
<tr>
<td>@ 10MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input 1 dB Comp. Point (High Gain)</td>
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<td>[dBm]</td>
</tr>
<tr>
<td>Input 1 dB Comp. Point (Low Gain)</td>
<td>-21</td>
<td>[dBm]</td>
</tr>
<tr>
<td>Power</td>
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<td>[mW]</td>
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<tr>
<td>Supply Voltage</td>
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<td>[V]</td>
</tr>
<tr>
<td>Technology</td>
<td>65 CMOS</td>
<td>[nm]</td>
</tr>
</tbody>
</table>

Summary & Conclusions

- mmWaves band offers a variety of new applications
- Technology scaling opened the opportunity to develop CMOS ICs working a tens of GHz
- Building blocks and transceivers demonstrated
- Big performance gap, compared to Radio Frequency ICs
- Further technology scaling will help but is not enough: the high operating frequency and CMOS limitations introduce many new challenges to circuits design
- Space for new ideas at all levels: device, circuit and architecture