A 4.8mW Inductorless CMOS Frequency Divider-by-4 with more than 60% Fractional Bandwidth up to 70GHz

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Outline

• Motivation

• Static versus dynamic CML latch

• Proposed differentially-driven dynamic CML latch

• Divider-by-4 based on proposed latches

• Experiments

• Conclusions
Injection-Locked Dividers for mm-Wave PLLs

- Limited power consumption
- Limited tunability and large inductor area

**but**
CML Static Dividers for mm-Wave PLLs

- Wide locking-range and small area
- Large power consumption and limited $f_{\text{MAX}}$ in CMOS

Ref -> PFD -> LPF -> $\div N$ -> mm-Wave prescaler

standard logic digital divider

$\div M$
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Initial condition at time $t_0$
- Input is High ($D > D_n$)
- Output is Low ($Q < Q_n$)
- $E$ switches from 0 to 1

$V_{out} = Q - Q_n$
Differential Pair as Dynamic CML Latch

The output state is momentarily stored on the load parasitic capacitance

\[ V_{\text{out}} = Q - Qn \]
Insight Into Dynamic Behavior: Read Phase

Small load resistance desirable to speed-up sensing phase

\[ m_1 = \frac{\Delta V}{RC} = \frac{I}{C} \quad m_2 = -\frac{\Delta V}{RC} = -\frac{I}{C} \quad \tau = RC \]
Insight Into Dynamic Behavior: Hold Phase

Large load resistance desirable to extend hold phase.

\[ m_1 = \frac{V_{DD} - V_Q(t_1)}{RC} \]
\[ m_2 = \frac{V_{DD} - V_{Qn}(t_1)}{RC} \]
\[ \tau = RC \]
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Proposed Differentially-Driven Latch (1)

Dynamically-modulated load resistance:
Small $R$ and high current for faster read phase

SD = Singly-Driven

$V_{out} = Q - Q_n$
Dynamically-modulated load resistance: Large R for longer hold phase

Proposed Differentially-Driven Latch (2)
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Dynamic Divider-by-4 Comparison: DD vs SD

Differentially-Driven Latches (DD)

Singly-Driven Latches (SD) *

*Presented at ISSCC 2011
Simulated Waveforms Close to SD $f_{MIN}$

Singly-Driven latch is almost completely discharged during the critical hold phase
Simulated Waveforms Close to SD $f_{\text{MAX}}$

Singly-Driven latch inverts the state just before the conclusion of the critical read phase.
Design trade-off: Locking-Range vs $f_0$

- All $L = 30\text{nm}$
- $P_{\text{diss}} \approx 2\text{mW}$
- $A_{\text{inSE}} = 250\text{mV}$
- Sinusoidal IN
Detailed Latch Design

Transistors’ size:

- $N_0$: $W = 8 \times 1\mu m$
- $N_1$: $W = 6 \times 1\mu m$
- $P_1$: $W = 4 \times 1\mu m$

All $L = 30$nm
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Technology:

32 nm LP
bulk CMOS
1V Supply
10 Cu layers

Realized by STMicroelectronics
Measured vs Simulated Sensitivity Curves
Measured Self-Oscillation Freq and $P_{DISS}$

- Self-oscillation freq (GHz)
- $\Delta V_{SG}$ pmos (mV)
- Power consumption (mW)
Comparison with the State of the Art

<table>
<thead>
<tr>
<th>Ref</th>
<th>div ratio</th>
<th>$f_{\text{MIN}}$-$f_{\text{MAX}}$ (GHz)</th>
<th>L.R. (%)</th>
<th>$P_{\text{DISS}}$ (mW)</th>
<th>Area ($\mu$m$^2$)</th>
<th>CMOS (nm)</th>
<th>FoM</th>
</tr>
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<tbody>
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<td>[1]</td>
<td>3</td>
<td>58.6-67.2</td>
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<td>37.4k</td>
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<td>62.9-71.6</td>
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<td>14 – $\geq 70$</td>
<td>$\geq 60$</td>
<td>$\leq 4.8$</td>
<td>990</td>
<td>32</td>
<td>$\geq 875$</td>
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</tbody>
</table>

$\text{FoM} = \text{L.R.} \times f_{\text{MAX}} / P_{\text{DISS}}$ (GHz/mW)

Conclusions

• Modulation of load resistance in dynamic CML latch improves L.R. up to 200%

• Up to 90% Locking Range in sub-bands for 0dBm input power

• Extremely wide tunability: input can span from 14 to 108GHz

• Low power consumption: 4.8mW @ 70GHz $f_{\text{IN}}$

• Core area only 18 x 55 $\mu$m$^2$