A 25Gb/s Low Noise 65nm CMOS Receiver tailored to 100GBASE-LR4

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Motivation

- Intensive utilization of high-speed optical communication calls for low cost solution (electronics part) → CMOS
Outline

- Existing approaches to high-speed receiver front-end
- Proposed two-stage front-end
- Receiver design
- Experiments
- Conclusions
100 GBASE-LR4 architecture

### TIA Requirement

<table>
<thead>
<tr>
<th></th>
<th>TIA Requirement</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise</td>
<td>$l_{in,\text{rms}} &lt; 4.2\mu\text{A rms}$</td>
<td>BER &lt; $10^{-12}$</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>~17GHz</td>
<td>$2/3 \times 25\text{Gb/s}$</td>
</tr>
<tr>
<td>Transimpedance gain</td>
<td>74dBΩ</td>
<td>300 mV$_{pp}$@RX output</td>
</tr>
</tbody>
</table>

- Target: low noise, wide bandwidth, significant gain
Low noise front-end: Common Gate TIA?

- Wide bandwidth needs large bias current, which degrades noise

\[
BW \approx \frac{1}{2\pi R_{\text{in}} C_{\text{tot, in}}} \approx \frac{g_{m_{M1}}}{2\pi C_{\text{tot, in}}}
\]

\[
I_{n,\text{in}}^2 \approx I_{n,M2}^2 + I_{n,R_D}^2 = 4kT \gamma g_{m_{M2}} + \frac{4kT}{R_D}
\]

\[
R_T = \frac{V_{\text{out}}}{I_{\text{in}}} \approx R_D \quad \text{(Transimpedance gain)}
\]
In low-speed shunt-feedback TIA, low noise achieved by large $R_F$
Shunt-feedback TIA: transimpedance limit

- \( A \cdot f_0 \): constant in a given technology node
- From transimpedance limit: \( R_F \sim 1/BW^2 \)
- Wide bandwidth results quite small \( R_F \), degrading noise significantly

\[
R_F \leq \frac{A \cdot f_0}{2\pi \cdot C_{\text{tot,in}} \cdot BW^2}
\]
Two-stage front-end: BW scaling

Conventional

Proposed
Two-stage front-end: noise reduction

- Noise of $R_F$: $1/n^2$
- Low frequency noise of Amp & EQ: $1/n^4$
- High frequency noise of Amp & EQ: not impacted
Input referred noise (n=2): $R_F$

$$S_{I,R_F} = \frac{4kT}{R_F n^2}$$

![Graph showing input referred noise](image)

- Conventional: \( \frac{4kT}{R_F} \)
- Proposed: \( \frac{4kT}{4R_F} \)

\( I_{n,in}^2 \) (dB/Hz) vs. \( \log f \) (Hz)
Input referred noise (n=2): amplifier

\[
S_{i,Amp} = \frac{S_{V,Amp}}{(R_F n^2)^2} \times \left| 1 + sR_F n^2 C_{tot,in} \right|^2
\]
Input referred noise (n=2): equalizer

\[ S_{I,\text{EQ}} = \frac{S_{V,\text{EQ}}}{|R_T(s)|^2} \]

\[ \bar{I}_{n,\text{in}}^2 \text{ (dB/Hz)} \]

\[ \frac{4kT\gamma}{gm_{\text{EQ}} \cdot R_F^2} \]

\[ \frac{4kT\gamma}{gm_{\text{EQ}} \cdot 16R_F^2} \]

24 dB/oct

16X

\[ \frac{BW}{2} \quad BW \quad \log f \text{ (Hz)} \]
Input referred noise (n=2): all

\[
S_{I,\text{total}} \approx S_{I,R_F} + S_{I,Amp} + S_{I,EQ} = \frac{4kT}{R_F n^2} + \frac{S_{V,Amp}}{(R_F n^2)^2} \left| 1 + sR_F n^2 C_{\text{tot,in}} \right|^2 + \frac{S_{V,EQ}}{R_T(s)}
\]
Comparison: noise (simulation)

- Optimal performance with $R_F$ of ~ 500 Ohm (noise vs. frequency response)
• 5-stage LA and 3-stage buffer provide sufficient gain

<table>
<thead>
<tr>
<th>Simulation*</th>
<th>Front-end</th>
<th>LA</th>
<th>Buffer</th>
<th>RX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (dB)</td>
<td>57.2</td>
<td>23.2</td>
<td>2.9</td>
<td>83.3</td>
</tr>
<tr>
<td>BW (GHz)</td>
<td>15.6</td>
<td>21.5</td>
<td>50</td>
<td>14.8</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>13.4</td>
<td>25.7</td>
<td>49.4</td>
<td>88.5</td>
</tr>
</tbody>
</table>

* Without photodiode
Low noise front-end

- Dummy mirror TIA: suppress common mode supply noise
- Push-pull amplifier: boosts open loop gain to 6.4, $R_F = 510\Omega$
- $R_F$ and $BW$ can be tuned independently for optimal performance
LA & Buffer gain stage

- Additional current load to boost Gm, formed by thick oxide transistor powered by higher Vdd (1.8V)
# Chip summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>ST 65nm Bulk CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core area</td>
<td>0.42 mm(^2) (0.66 x 0.64)</td>
</tr>
<tr>
<td>Power consumption</td>
<td>93 mW</td>
</tr>
<tr>
<td>Voltage supply</td>
<td>1 / 1.8 V</td>
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</table>

![Chip Image]

- Technology: ST 65nm Bulk CMOS
- Core area: 0.42 mm\(^2\) (0.66 x 0.64)
- Power consumption: 93 mW
- Voltage supply: 1 / 1.8 V
Frequency response

S21, S11 (single-ended); S22, Z21 (differential)

<table>
<thead>
<tr>
<th>Item</th>
<th>Nominal</th>
<th>Tuning</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_T$ (dBΩ)</td>
<td>83</td>
<td>78 ~ 87.1</td>
</tr>
<tr>
<td>Bandwidth (GHz)</td>
<td>13.6*</td>
<td>10.6 ~ 18.2</td>
</tr>
</tbody>
</table>

* Pure electrical, which becomes 17 GHz at 80fF PD cap + 0.5nH bondwire (sim.)

Single-ended in, differential out

$$Z_T = \frac{Z_0(S_{21} - S_{31})}{1 - S_{11}}$$
Input referred noise current spectral density

- $I_{n,rms} = 2.44 \mu A_{rms}$, $I_{n,\text{ispectrum,avg}} = 20.9 pA \sqrt{\text{Hz}}$
Electrical eye diagram plot

- Electrical eye diagram with $\sim 14\text{mV}_{pp}$ input voltage (after attenuation)
- Eye amplitude: $662\text{mV}_{pp}$, Jitter$_{rms} = 2.5\text{ps}$ (PRBS31)
## Comparison

<table>
<thead>
<tr>
<th>Ref.</th>
<th>This Work</th>
<th>CICC10</th>
<th>JSSC08</th>
<th>JSSC12</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS Tech. (nm)</td>
<td>65</td>
<td>65</td>
<td>90</td>
<td>45 (SOI)</td>
</tr>
<tr>
<td>Bit Rate (Gb/s)</td>
<td>25</td>
<td>25</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>Bandwidth (GHz)</td>
<td>13.6</td>
<td>22.8*</td>
<td>22</td>
<td>30</td>
</tr>
<tr>
<td>Transimpedance (dBΩ)</td>
<td>83</td>
<td>69.8*</td>
<td>66</td>
<td>55</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>1 / 1.8</td>
<td>1 / 1.8</td>
<td>1.2</td>
<td>1</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>93</td>
<td>74</td>
<td>75</td>
<td>9</td>
</tr>
<tr>
<td>Noise (pA/√Hz)</td>
<td>20.9***</td>
<td>-</td>
<td>22**</td>
<td>20.5</td>
</tr>
<tr>
<td>FOM (GHz·Ω/mW)</td>
<td>2066</td>
<td>952</td>
<td>585</td>
<td>1874</td>
</tr>
</tbody>
</table>

*: simulated, **: differential, ***: including dummy mirror TIA

- Highest FOM obtained
Conclusions

- A 25 Gb/s optical receiver in 65nm CMOS presented, meeting 100GBASE-LR4 with margin
- A new low noise technique proposed: noise and BW trade-off broken by two-stage front-end architecture
- Low noise achieved with state-of-the-art FOM