A 5mW CMOS Wideband mm-Wave Front-End Featuring 17dB of Conversion Gain and 6.5dB Minimum NF

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RTU2D-5
Phased-array receiver architecture

Overall receiver:

\[
G_{\text{tot}} = M G_0 \\
F_{\text{tot}} = \frac{F_0 - 1}{M} + 1
\]

Pros:
- Steerable directive antenna

Cons:
- M times area and power consumption

A compact and low-power front-end is highly desirable in this framework
Outline

• Limits of conventional mm-wave LNAs
• Proposed front-end solution
• Performance analysis and discussion
• Experimental results
• Conclusions
Conventional mm-wave LNAs

- $R_P = Q/(\omega_0 C_P)$
- $A_{\text{stage}} = g_m R_P \geq 3 \quad \text{dB}$
- Gain limited by low $R_P$ at mm-Wave
- Noise contributed by cascaded stages is significant
- Wide area
- Large $P_{\text{DISS}}$
- Narrow BW
Proposed front-end

\[ A_{\text{MATCH}} = \frac{V_G}{V_S} \quad 5 \quad 7\text{dB} \quad \frac{I_{RF}}{V_S} = A_{\text{MATCH}} g_m \]

- No inefficient I-V conversions at mm-Wave
- A single matched \( g_m \) stage can provide enough gain to suppress the noise of the following stages
- I-V conversion performed at IF where \( R_P \) is larger
Noise at the image band

![Diagram of a radio frequency integrated circuit (RFIC) with labels for RF input, LO, RF, IF, and image frequency bands. The diagram includes a multistage LNA and a single-stage trans-G.](image)
Rejection of the image noise
Circuit implementation

$n_{1,2}$: 20µm/60nm

$p_1$: 36µm/180nm

$L_G$: 330pH

$C_{pad}$: 70fF

$L_F$: 225pH

$C_F$: 290fF

$L_L$: 770pH

$n_1$ biased for optimum $f_{max}$: $I_D/W = 250\mu A/\mu m$

low DC current in $n_2$ for low noise and fast switching
Image reject filter

Series resonance: rejects the image

Parallel resonance: cancels $C_P$ and raises gain

- Series resonance:
  \[ \omega_z = \frac{1}{\sqrt{L_F C_F}} \]

- Parallel resonance:
  \[ \omega_p = \frac{1}{\sqrt{\frac{L_F}{C_F + C_P} \cdot \frac{C_F C_P}{C_F + C_P}}} \]
Noise comparison with cascode LNA

Same transistors’ size and $P_{\text{DISS}}$

<table>
<thead>
<tr>
<th></th>
<th>NF (dB)</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LNA</td>
<td>5.3</td>
<td>11.5</td>
</tr>
<tr>
<td>mixer w/o rej</td>
<td>7.7</td>
<td>16.5</td>
</tr>
<tr>
<td>mixer with rej</td>
<td>6.0</td>
<td>18.0</td>
</tr>
</tbody>
</table>

RFIC – Montréal June 17-19, 2012
Comparison with cascaded LNA & mix

Same transistors’ size and current density

<table>
<thead>
<tr>
<th></th>
<th>NF (dB)</th>
<th>Gain (dB)</th>
<th>$P_{\text{DISS}}$ (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>mixer</td>
<td>6.0</td>
<td>18.0</td>
<td>5.0</td>
</tr>
<tr>
<td>2 stages</td>
<td>7.3</td>
<td>20.1</td>
<td>10</td>
</tr>
</tbody>
</table>

The proposed solution has better NF and linearity, larger RF bandwidth and similar gain while saving remarkable area and power consumption
Technology:
CMOS 65nm

Core area:
0.054mm²

Power:
5mW

Supply voltage:
1V

Test chips realized by STMicroelectronics
Measured $S_{11}$

Front-end is matched (i.e. $S_{11} \leq -10\text{dB}$) from 52.5 to 62.5GHz
17 dB peak gain and 6.5 dB min NF over ≥ 3.5 GHz -3 dB BW

Gain

NF

$\text{f}_{\text{LO}} = 37 \text{GHz}$
17dB peak gain and 6.5dB min NF over ≥ 14GHz -3dB BW

Gain

NF

\( f_{\text{IF}} = 18.5\text{GHz} \)
## Performance summary

<table>
<thead>
<tr>
<th>Tech. CMOS</th>
<th>Weyers ISSCC 2008</th>
<th>Pellerano JSSC 2008</th>
<th>Yao JSSC 2007</th>
<th>Cohen RFIC 2008</th>
<th>Heidari JSSC 2007</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>f₀ (GHz)</td>
<td>60</td>
<td>64</td>
<td>58</td>
<td>58</td>
<td>63</td>
<td>54</td>
</tr>
<tr>
<td>RF BW (GHz)</td>
<td>7.7</td>
<td>8.0</td>
<td>8.2</td>
<td>5.0</td>
<td>4.5</td>
<td>14</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>22.3</td>
<td>15.5</td>
<td>14.6</td>
<td>15.0</td>
<td>12.2</td>
<td>17.0</td>
</tr>
<tr>
<td>NFₘᵣₙ (dB)</td>
<td>6.1</td>
<td>6.5</td>
<td>5.0</td>
<td>4.4</td>
<td>5.5</td>
<td>6.5</td>
</tr>
<tr>
<td>1dB cp (dBm)</td>
<td>-20</td>
<td>-12</td>
<td>-16</td>
<td>-18</td>
<td>-8.2</td>
<td>-9.0</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.080</td>
<td>0.520</td>
<td>0.100</td>
<td>0.085</td>
<td>0.360</td>
<td>0.055</td>
</tr>
<tr>
<td>Pₐₛₛₜ (mW)</td>
<td>35</td>
<td>86</td>
<td>24</td>
<td>3.9</td>
<td>11</td>
<td>5.0</td>
</tr>
<tr>
<td>FoM (GHz)</td>
<td>0.08</td>
<td>0.09</td>
<td>0.14</td>
<td>0.76</td>
<td>1.24</td>
<td>2.78</td>
</tr>
</tbody>
</table>

FoM = (Gain * 1dBcp * f₀) / ((F-1) * Pₐₛₛₜ)
Conclusions

• Single-stage stacked LNA-mixer has been presented
• No resonant load at RF leads to very wide RF bandwidth
• Notch filtering at image frequency enhances gain and lowers NF
• The front-end shows remarkable power and area saving
• Optimized for sliding-IF phased array receivers