A 33.6-46.2GHz 32nm CMOS VCO with 177.5dBc/Hz minimum noise FoM using inductor splitting for tuning extension

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Mm-wave VCOs - issues

- Tuning Range reduces dramatically
- Wide Tuning Range leads to poor phase noise FoM
- State of the art FoM and wide tuning range is challenging
Review of switched capacitor tuning

- $C_{\text{FIX}}$: parasitic cap of buffer and core devices
- $C_{\text{FIX}}$ equal or greater than $C_T$ at mmWave

- SW ON: $f_{\text{MIN}} = \frac{1}{2\pi \sqrt{L_T (C_{\text{FIX}} + C_T)}}$

- SW OFF: $f_{\text{MAX}}$ determined by $C_{\text{FIX}}$

\[
f_{\text{MAX}} = \frac{1}{2\pi \sqrt{L_T \left( C_{\text{FIX}} + \frac{C_T C_{\text{SW}}}{C_T + C_{\text{SW}}} \right)}} \quad \text{for} \quad C_{\text{SW}} \ll C_T, C_{\text{FIX}}
\]

\[
\rightarrow \frac{1}{2\pi \sqrt{L_T C_{\text{FIX}}}}
\]
Proposed switched capacitor tuning

- \( c_{SW} \) in series with \( C_T + C_{FIX} \)
- Much higher frequency jump

\[ f_{\text{MAX}} = \frac{1}{2\pi \sqrt{L_T \frac{(C_T + C_{FIX})c_{SW}}{C_T + C_{FIX} + c_{SW}}}} \]

\( c_{SW} \ll C_T, C_{FIX} \)

\[ \rightarrow \frac{1}{2\pi \sqrt{L_T c_{SW}}} \]

- SW ON: \( f_{\text{MIN}} \) as in switched cap. oscillator
- SW OFF: \( C_{FIX} \) no more limiting

Mammei et al., ISSCC 2013
Comparison with same frequency jump

Assuming: $C_{\text{FIX}} = C_T = 100\, \text{fF}$, $L_T = 100\, \text{pH}$, $\text{FOM}_{SW} = 550\, \text{fs}$

$f_{\text{MIN}} = 35.6\, \text{GHz}$, $f_{\text{MAX}} / f_{\text{MIN}} = 1.2$

Switch off

- $W_{\text{sw}} = 41\, \mu\text{m}$, $c_{SW} = 50\, \text{fF}$
  - $r_{SW} = 11\, \Omega$, $Q = 8$

- $W_{\text{sw}} = 330\, \mu\text{m}$, $c_{SW} = 400\, \text{fF}$
  - $r_{SW} = 1.37\, \Omega$, $Q = 16$

Switch on
$Q$ vs $f_{\text{max}}/f_{\text{min}}$ with finite components $Q$

Advantage increase for higher frequency step and/or larger $C_{\text{fix}}$
- Inductor splitting with $M_{SW}$ for the largest tuning step
- Variable tank capacitance ($C_T$) with switched digital MOMs and varactor
- $L_T=100\,\mu\text{H}, C_T=140\,\text{fF}, C_{\text{FIX}}\approx120\,\text{fF}$
- Tank Q ranges from 4 to 5.5
- Transformer feedback avoids latching when $M_{SW}$ is off
- $R_b$ instead of current mirrors lowers 1/f noise
Test Chip

- CMOS 32nm LP from STMicroelectronics
- Core Area 70um x 120um
- 40GHz center frequency

- Phase Noise measured after divider by 4 in X-Band (8-12GHz)
- 9.8mW from 1V supply
Phase Noise & FoM over Tuning Range

![Graph showing Phase Noise and FoM over Frequency range with M_sw ON and M_sw OFF at 10 MHz offset.](image)
### Summary and Comparison

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*estimated from the reported phase noise at 1MHz*
Outline

- VCO Design in ultra scaled technology
- Analysis of the proposed resonator
- Test chips design and experimental results
- Conclusions
CMOS Technology Evolution

- Continuous scaling driven by complex Systems on Chip
- ~20-30% $f_T$ improvement only per generation
- mmWave passive components penalty due to BEOL scaling
CMOS 65nm vs 32nm: BEOL

- 32nm H.L.M closer to substrate (~85%) but same thickness
- 32nm L.L.M. closer to substrate and thinner (~50%)
- 2 time resistivity of 32nm VIAs
Performance of MOS Switches

- Trade-off between $c_{sw}$ and $r_{sw}$
- $FOM_{sw}$ measures quality of the switch:
  
  $$FOM_{sw} = C_{OFF} \cdot R_{ON} \propto \frac{1}{f_T}$$

$$r_{sw} \propto \frac{1}{g_m}$$

$$c_{sw} \propto C_{GS}$$
• Routing parasitics comparable to $r_{SW}$ and $c_{SW}$

• FOM tends to saturate in ultra scaled technologies
Inductors usually realized with top metals for maximum Q and self Resonance frequency

Slightly lower dielectric constant in 32nm compensates lower metal distance to substrate in 32nm
CMOS 65nm vs 32nm: MOM Capacitors

MOM capacitors realized with low level metals for max. density

MOM Q in 32nm ~70% than 65nm due to half thickness of LLM and 2x via resistance
Evidenziate con una caption qual è la misura e quale la simulazione

Frank; 19/01/2013
Switched Capacitor Tank

- Transistors Switch FOM, saturating in ultra scaled technologies, determines the trade off between Tuning Range and $Q$
- Significant MOM loss ($R_{MOM}$) due to higher metals and vias resistivity
- Switched cap. tank does not benefit from technology scaling

$$Q_{low} = \frac{2}{\omega C_{MOM}(2R_{MOM} + r_{SW})}$$

$$\frac{C_{MAX}}{C_{MIN}} = \frac{C_{MOM}}{2c_{SW}} + 1$$
Q versus $C_{\text{MAX}}/C_{\text{MIN}}$

32nm switched MOM slightly worse than 65nm

![Graph showing Q versus $C_{\text{MAX}}/C_{\text{MIN}}$ with lines for CMOS65nm and CMOS32nm at 40GHz.](image)
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Switched Cap. Oscillator

- $C_{FIX}$: buffer parasitic and core devices
- $C_{FIX}$ equal or greater than $C_T$ at mmW

**SW ON**

$$f_{MIN} = \frac{1}{2\pi \sqrt{L_T (C_{FIX} + C_T)}}$$

**SW OFF:** $f_{MAX}$ determined by $C_{FIX}$

$$f_{MAX} = \frac{1}{2\pi \sqrt{L_T \left( C_{FIX} + \frac{C_T C_{SW}}{C_T + C_{SW}} \right)}} \rightarrow \frac{1}{2\pi \sqrt{L_T C_{FIX}}},$$
Proposed Oscillator

\[ f_{\text{MAX}} = \frac{1}{2\pi \sqrt{L_T \left( \frac{(C_T + C_{\text{FIX}})c_{\text{SW}}}{C_T + C_{\text{FIX}} + c_{\text{SW}}} \right)}} \]

- \( c_{\text{SW}} \) in series with \( C_T + C_{\text{FIX}} \)
- Higher frequency jump

- SW.ON: \( f_{\text{MIN}} \) as in switched cap. oscillator

- SW.OFF: \( C_{\text{FIX}} \) no more limiting \( f_{\text{MAX}} \)
Comparison for the Same Frequency Jump

Assuming: \( C_{\text{FIX}} = C_T = 100\text{fF}, \ L_T = 100\text{pH}, \ \text{FOM}_{\text{SW}} = 550\text{fs} \)
\( f_{\text{MIN}} = 35.6\text{GHz}, \ f_{\text{MAX}}/f_{\text{MIN}} = 1.2 \)

\[ c_{\text{SW}} = 50\text{fF} \]
\[ c_{\text{SW}} = 400\text{fF} \]

For the same frequency step, switch in the proposed tank may display much larger \( c_{\text{SW}} \)
Comparison for the Same Frequency Jump

Assuming: \( C_{\text{FIX}}=C_T=100\,\text{fF}, \; L_T=100\,\text{pH}, \; \text{FOM}_{SW}=550\,\text{fs} \)
\( f_{\text{MIN}}=35.6\,\text{GHz}, \; f_{\text{MAX}}/f_{\text{MIN}}=1.2 \)

\[ \begin{align*}
\text{c}_{SW} &= 50\,\text{fF} \\
r_{SW} &= 11\,\Omega \\
Q &= 8
\end{align*} \]

\[ \begin{align*}
\text{c}_{SW} &= 400\,\text{fF} \\
r_{SW} &= 1.37\,\Omega \\
Q &= 16
\end{align*} \]

Much lower \( r_{SW} \) leads to 2x tank Q
Scrivi Ohm per rsw. Perché 2x improvement?

Frank, 19/01/2013
Advantage increases for higher frequency step and/or larger $C_{fix}$. 

Proposed Tank

Switch Capacitor

@40GHz
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• VCO Design in ultra scaled technology
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Loop Gain with a conventional transconductor

\[ G_{\text{LOOP}} = g_m R_P \]

Switch ON

\[ R_{PON} = \omega L_T Q_T \]

Switch OFF

\[ R_{POFF} = \omega L_T Q_T \alpha^2 \]

\[ \alpha = \frac{c_{sw}}{C_T + C_{FIX} + c_{sw}} = 0.55 \div 0.75 \]

- Loop gain penalty
- Tank is an open at DC, latching issue
Loop Gain with Transformer Feedback

\[ G_{\text{LOOP}} = g_m Z_{21} \]

\[ Z_{21} = K \sqrt{\frac{L_S}{L_T}} R_{\text{PON}} \]

Switch ON

\[ Z_{21} = K \sqrt{\frac{L_S}{L_T}} \frac{R_{\text{POFF}}}{\alpha} \]

\[ \alpha = \frac{c_{sw}}{C_T + C_{\text{FIX}} + c_{sw}} = 0.55 \div 0.75 \]

Switch OFF

- Transformer restores loop gain and avoids latching

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Simulated Impedance $R_P$ and $Z_{21}$

![Graph showing simulated impedance $R_P$ and $Z_{21}$ as functions of frequency.](image)
Spec for a 60GHz Sliding IF Architecture

- first down-conversion to 1/3 the received frequency
- quadrature down-conversion to DC

- 40 GHz VCO center frequency with more than 20% T.R.
- Phase Noise @ 10MHz offset better than -115dBc/Hz
Realized VCO

- Inductor splitting with $M_{SW}$ for largest tuning step
- Variable tank capacitance ($C_T$) with switched digital MOMs and varactor
  - $L_T=100\mu$H, $C_T=140\text{fF}$, $C_{FIX}=120\text{fF}$
  - Tank Q ranges from 4 to 5.5
- $R_b$ instead of PMOS mirrors lowers $1/f$ noise
Chip Blocks Diagram

- Direct output and after div. by 4 for Phase Noise measurement in X-Band (8-12GHz)
- CMOS 32nm LP from STMicroelectronics
- Supply voltage: 1V
- Core area: 70um x 120um
40GHz Phase Noise Measurement

![Phase Noise vs Frequency Offset Graph]

- **Phase Noise [dBc/Hz]**
- **Frequency Offset [Hz]**

- **$1/f^3$**
- **$1/f^2$**
Phase Noise and FoM over Tuning Range

![Graph showing phase noise and FoM over frequency range with M_sw ON and OFF]

- Phase Noise [dBc/Hz]
- FOM [dBc/Hz]
- Frequency [GHz]
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Conclusions

• Design of mmW VCOs does not benefit from ultra scaled technologies. BEOL scaling increases routing parasitics and loss of MOM capacitors.

• A new switched resonator circuit topology, improving Q for large frequency tuning step, has been presented.

• A 40 GHz VCO in 32nm CMOS has been presented. Measurements proved a state of the art FOM over a very large tuning range.