Insights Into Circuits for Frequency Synthesis at mm-Waves

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High data rate wireless networks

- ~7GHz of unlicensed bandwidth available around ~60GHz
- Intense standardization activity
  - WiGig, 802.11ad, WirelessHD, 802.15.3c, ECMA-387
Outline

• **Frequency synthesizer for a sliding-IF mmWave Receiver in 65nm CMOS**

• Inductor-less CMOS frequency divider operating up to 70GHz

• A low-noise wide tuning-range mmWave VCO in 32nm CMOS

For more refer to:
PHY for Gb/s wireless communications

- High Rate 60GHz PHY Proposal

- Large RF bandwidth (~9GHz minimum)
- RX Minimum Sensitivity: from -60dBm (1Gb/s) to -50dBm (4Gb/s)
- RX Maximum Noise Figure < 10dB
- Large LO tuning range required
- Very stringent phase noise at maximum data rate

Phase noise requirements

- Phase noise rotates signal constellation and impairs BER
- Phase noise $<-113$dBc/Hz @10MHz is required in most stringent cases, assuming 1MHz PLL bandwidth

Source: IEEE 802.15-06-0477-01-003c [Online]
Sliding-IF RX architecture

- First down-conversion to 1/3 of the received frequency
  - Only one PLL at 38.9\text{GHz} \div 43.2 \text{GHz}
  - Integrated PN: < -20\text{dBc}
- Dividers by 2 to generate I/Q IF signals
PLL architecture

36 MHz

PFD → CP → VCO

CP contribution to In-band phase noise:

\[ L_{CP} = \frac{S_{Icp}}{2 \frac{I_{CP}}{2\pi} \frac{1}{N^2}} \]

- Design strategy
  - Increase CP current (2mA)
  - *But* reduce VCO gain (500MHz/V)
  - *And* optimize LPF to ensure stability

*Increasing I_{CP} reduces L_{CP} but stability becomes an issue*
40GHz VCO and Dividers

16% Tuning Range

~ 30% Locking Range
Phase Noise Measurements

- VCO Phase Noise:
  - $-118.5\text{dBc/Hz @10MHz}$ from 40 GHz carrier

- Integrated Phase Noise:
  - $-22.5\text{dBc [10kHz-10MHz]}$ from 60GHz carrier
mmWave receiver

- Technology: STM 65nm CMOS
- Area: 2.4mm²
- Power Consumption:
  44mW PLL, 40mW RX front-end

Gain (dB)

Noise Figure (dB)

Frequency (GHz)

57-66 GHz

External LO
- Integrated PLL
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For more, refer to:
A. Ghilioni et al., “*mm-wave frequency dividers analysis and design based on dynamic latches with load modulation*” JSSC August 2013
Injection locked LC dividers

- Many examples demonstrated on bulk CMOS
- Limited tunability due to the LC resonance
- Trade off between bandwidth (tank Q) and power consumption
- Large area due to the inductor
CML static dividers for mmW PLLs

- Very wide operating range
- Small area (no inductors)
- Large power consumption to reach mm-Waves
Brief review on static CML latch

- $M_{1-2}$ sense the input when $E$ is High
- $M_{3-4}$ regenerative pair stores the sampled data during hold

\[ V_{\text{out}} = Q - Q_n \]
• Regenerative pair is removed
• The sampled data is temporarily stored on the load (parasitic) capacitors

A. Ghilioni et al., ISSCC 2011
Diff. pair as a dynamic CML latch

- Design trade-off for selection of the load resistance

  - Read phase:
    - Small load resistance desirable to speed-up sensing phase
    - Large load resistance desirable to extend hold phase

  - Hold phase:
    - Large load resistance desirable to extend hold phase

A. Ghilioni et al., ISSCC 2011
Dynamic latch with load modulation

- **READ**
  - Small R and high current for faster read phase
  - No load modulation

- **HOLD**
  - Large R for longer hold phase
  - No load modulation
Synchronous divider by four

~2x wider bandwidth with load modulation

no load modulation
load modulation
Simulated Waveforms

Output waveforms of a latch at min and max operating frequency of the version without load modulation:

@ fmin

no load modulation

with load modulation

@ fmax
Test chip photomicrograph

- Technology: 32nm bulk CMOS
- Core area: 18 x 55 µm²
- Supply voltage: 1V
Meas vs. sim: sensitivity curves
Measured phase noise

![Graph showing measured phase noise](image)

**Phase noise** [-dBc/Hz]

**Frequency offset from carrier** [Hz]

- PSG
- Divider's output
## Comparison with state of the art

<table>
<thead>
<tr>
<th>Ref</th>
<th>$f_{in}/f_{out}$</th>
<th>$f_{min}$-$f_{max}$ (GHz)</th>
<th>L.R. (%)</th>
<th>$P_{diss}$ (mW)</th>
<th>Area ($\mu m^2$)</th>
<th>Tech CMOS (nm)</th>
<th>FoM (GHz/mW)</th>
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<tr>
<td>[6]</td>
<td>3</td>
<td>58.6-67.2</td>
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<td>58.5-72.9</td>
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<td>6.55</td>
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<td>$14^b$ – $70^c$</td>
<td>60 – 90</td>
<td>$1.3$ – $4.8$</td>
<td>$18 \times 55$</td>
<td>32</td>
<td>$6.67$ – $17.5$</td>
</tr>
</tbody>
</table>
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- Inductor-less CMOS frequency divider operating up to 70GHz
- A low-noise wide tuning-range mmWave VCO in 32nm CMOS

For more, refer to:
E. Mammei et al., “A 33.6-to-46.2GHz 32nm CMOS VCO with 177.5dBc/Hz minimum noise FOM using inductor splitting for tuning extension” ISSCC 2013
Issues of mmWave - VCOs

- Tuning Range reduces dramatically at mmWave
- High Tuning Range leads to poor phase noise FoM
- Achieving state of the art FoM and wide tuning range is challenging
Improvement from tech. scaling?

- Continuous scaling driven by complex Systems on Chip
- ~20-30% $f_T$ improvement only per generation
- Aggressive scaling of BEOL:
  - Large impact of routing parasitic (layout)
  - Passive components penalty

[Graph showing cut-off frequency vs. drain current density with data points for 32 nm, 45 nm, 65 nm, and 90 nm process nodes.]

IEDM 2010, S. Francisco
CMOS 65nm vs 32nm: BEOL

- 32nm H.L.M closer to substrate (~85%) but same thickness
- 32nm L.L.M. closer to substrate and thinner (~50%)
- 2x resistivity of 32nm VIAs
Performance of switches

\[ r_{SW} \propto \frac{1}{g_M} \]

\[ c_{SW} \propto C_{GS} \]

\[ FOM_{SW} = c_{SW} \cdot r_{SW} \propto \frac{1}{f_T} \]

Considering post-layout, mild advantage beyond 45nm
65nm vs 32nm: passives

Slightly lower dielectric constant in 32nm compensates lower metal distance to substrate

MOM Q in 32nm ~70% than 65nm due to half thickness of LLM and 2x via resistance

CMOS 65nm

CMOS 32nm

L=100pH

CMOS 65nm

C=250fF

CMOS 32nm
32nm switched MOM slightly worse than 65nm
Review of switched capacitor tuning

- $f_{\text{MIN}} = \frac{1}{2\pi\sqrt{L_T\left(C_{\text{FIX}} + C_T\right)}}$

- $f_{\text{MAX}} = \frac{1}{2\pi\sqrt{L_T\left(C_{\text{FIX}} + \frac{C_T c_{SW}}{C_T + c_{SW}}\right)}}$

- $f_{\text{MAX}} \leq \frac{1}{2\pi\sqrt{L_T C_{\text{FIX}}}}$

- $C_{\text{FIX}}$: parasitic cap of buffer and core devices

- $C_{\text{FIX}} \geq C_T$ at mmWave

- SW OFF: $f_{\text{MAX}}$ determined by $C_{\text{FIX}}$

- SW ON: $f_{\text{MAX}}$ determined by $C_{\text{FIX}}$
Proposed switched capacitor tuning

- \( c_{SW} \) in series with \( C_T + C_{FIX} \)
- Much higher frequency jump

- SW ON: \( f_{MIN} \) as in switched cap. oscillator
- SW OFF: \( C_{FIX} \) no more limiting \( f_{MAX} \)

\[
f_{MAX} = \frac{1}{2\pi \sqrt{L_T \frac{(C_T + C_{FIX})c_{SW}}{C_T + C_{FIX} + c_{SW}}}} \quad \text{if} \quad c_{SW} \ll C_T, C_{FIX} \quad \Rightarrow \quad \frac{1}{2\pi \sqrt{L_T c_{SW}}}
\]
Comparison with same frequency jump

Assuming: $C_{\text{FIX}}=C_T=100\, \text{fF}$, $L_T=100\, \text{pH}$, $\text{FOM}_{SW}=550\, \text{fs}$

$f_{\text{MIN}}=35.6\, \text{GHz}$, \quad $f_{\text{MAX}}/f_{\text{MIN}}=1.2$

\begin{align*}
W_{\text{sw}} &= 41\, \mu\text{m}, \quad c_{\text{SW}}=50\, \text{fF} \\
W_{\text{sw}} &= 330\, \mu\text{m}, \quad c_{\text{SW}}=400\, \text{fF}
\end{align*}

Switch off

\begin{align*}
r_{\text{SW}} &= 11\, \Omega, \quad Q=8 \\
r_{\text{SW}} &= 1.37\, \Omega, \quad Q=16
\end{align*}

Switch on
Q vs $f_{\text{max}}/f_{\text{min}}$ with finite components Q

Advantage increase for higher frequency step and/or larger $C_{\text{fix}}$
VCO Design

- Inductor splitting with $M_{SW}$ for the largest tuning step
- Variable tank capacitance ($C_T$) with switched digital MOMs and varactor
- $L_T=100\,\text{pH}$, $C_T=140\,\text{fF}$, $C_{FIX}\approx120\,\text{fF}$
- Tank Q ranges from 4 to 5.5
- Transformer feedback avoids latching when $M_{SW}$ is off
- $R_b$ instead of current mirrors lowers $1/f$ noise
Test Chip

- CMOS 32nm LP from STMicroelectronics
- Core Area 70um x 120um
- 40GHz center frequency

- Phase Noise measured after divider by 4 in X-Band (8-12GHz)
- 9.8mW from 1V supply
Phase Noise & FoM

10 MHz offset

Phase Noise [dBc/Hz]

FOM [dBc/Hz]

Frequency [GHz]
# Summary and Comparison

<table>
<thead>
<tr>
<th>REF</th>
<th>FREQ [GHz]</th>
<th>TR [%]</th>
<th>POWER [mW]</th>
<th>PN @10MHz [dBc/Hz]</th>
<th>FOM [dBc/Hz]</th>
<th>TECH</th>
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<tr>
<td>CICC12</td>
<td>57.5/90.1</td>
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<td>33.6/46.2</td>
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<td>-115.2/-118</td>
<td>177.5/180</td>
<td>32nm</td>
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</table>
Conclusions

• A 65nm PLL proves suitable to satisfy the stringent requirements of a wideband mmW receiver, exploiting the advantages of a sliding IF RX architecture.

• Key PLL building blocks have been investigated to improve synthesizer performances in ultra-scaled CMOS nodes:
  ✓ a compact divider by-4 based on dynamic latches with > 60% fractional bandwidth, < 5mW power, 55x18μm²
  ✓ a 40GHz VCO with 31% T.R, 10mW power and a remarkable phase noise FOM > 177.5dBc/Hz.
References

- [3] A. Ghilioni et al.: “A 4.8mW inductorless CMOS Frequency Divider-by-4 with more than 60% Fractional Bandwidth up to 70GHz” in Proceedings of the IEEE Custom Integrated Circuits Conference (CICC), San Jose (California, USA), September 2012
References