A 15 GHz Bandwidth 20 dBm $P_{\text{SAT}}$
Power Amplifier
with 22% PAE in 65 nm CMOS

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Outline

• Wideband Power Amplifier Design Challenges
• Coupled Resonators to Improve GBW
• Wideband Power Combining/Splitting
• Circuit Design and Measurement
• Conclusions
Wideband Power Amplifier Design Challenges

- High efficiency requires high gain

\[
PAE = \frac{P_{Out} - P_{In}}{P_{DC}} = \frac{P_{Out}}{P_{DC}} \left(1 - \frac{1}{G}\right)
\]

- Bandwidth trades with gain and efficiency
- Improving GBW is the key to achieve high efficiency over large bandwidth
GBW of Power Amplifiers

- **Active devices**
  - Maximum gain is limited by technology
  - Class AB biasing further reduces gain
  - Large layouts determine significant parasitics

- **Passive matching networks**
  - High-order networks can enhance GBW
  - Compact layout to minimize loss
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Coupled Resonators

- Simple topology and low loss
- Two peaking frequencies:

\[ \omega_L \approx \frac{1}{\sqrt{LC}}, \quad \omega_H \approx \sqrt{1 + 2 \frac{L}{L_C}} \omega_L \]

- \( L_C \) used to control the bandwidth

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Coupled resonators allow 2x GBW enhancement (GBWEN)
Transformation of Coupled Resonators

\[ GBW_{EN} = \frac{n + 1}{\sqrt{n}} \geq 2 \]
Effect of Layout Parasitics

- Limited inductor Q leads to asymmetric response
- Network needs to be smart to accommodate parasitics

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Restoring Flat Response

- Coupled resonator can be conveniently tuned to achieve flat response

\[
\left| \frac{Z_T(\omega_H)}{Z_T(\omega_L)} \right| \approx \frac{L_1}{L_3}
\]

\begin{figure}
\centering
\includegraphics[width=\textwidth]{figure}
\caption{Increasing $L_1/L_3$}
\end{figure}

Q=10

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Power Combing

- Power combining is mandatory to achieve high Pout for CMOS PAs

- Transformer based combiner/splitter is popular
  - Compact size
  - Low insertion loss
  - Generally narrow bandwidth

- Wideband combining through coupled resonators
Wideband Combiner

- Easy to transform
- Divide the left network into two equal portions

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Wideband Splitter

(a) conventional coupled resonators

(b) power splitter using coupled resonators

- Easy to transform
- Divide the right network into two equal portions
Comparison with Transformer Splitter

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(a) transformer based splitter

(b) proposed splitter

More than two times GBW enhancement.
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PA Design

- A prototype has been designed in ST 65nm CMOS
  - Bandwidth >13 GHz
  - Gain > 25dB
  - P1dB > 15dBm
  - PAE > 20%

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Layout of Splitter

- Two different layout topologies for splitter

(a) splitter network

(b) 1\textsuperscript{st} topology

(c) 2\textsuperscript{nd} topology
Stability Analysis

- Proposed splitter can suppress differential-mode common-mode oscillation

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Measured S-Parameters

Gain ≈ 30 dB, \( BW_{3dB} : 58.5-73.5 \text{GHz} \)

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Large Signal Performances at 65GHz

\[ P_{\text{SAT}} \approx 20 \text{dBm}, \quad P_{1\text{dB}} \approx 16 \text{dBm}, \quad \text{PAE} \approx 22\% \]
Large Signal Performances over Frequency

\[ P_{\text{Sat}} > 19 \text{dBm}, \quad P_{1\text{dB}} > 15 \text{dBm}, \quad \text{PAE} > 15\% \text{ over the bandwidth} \]
Performance Summary and Comparison

<table>
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<tr>
<th>Reference</th>
<th>Tech. &amp; Vdd</th>
<th>Gain (dB)</th>
<th>BW (GHz)</th>
<th>GBW (GHz)</th>
<th>P_{SAT} (dBm)</th>
<th>P_{1dB} (dBm)</th>
<th>PAE (%)</th>
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</table>

State-of-the-art $P_{SAT}$ and PAE with the largest GBW
Conclusions

• High GBW is critical for high efficient, wideband PAs

• Coupled resonators can improve PA GBW while keeping compact layout

• A methodology has been proposed to design wideband combiner/splitter using coupled resonators

• A three-stage two-path PA with 20dBm $P_{\text{SAT}}$, 22% PAE, and 15GHz bandwidth in 65nm CMOS was demonstrated
Acknowledgements

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Thank You!
References

[1] A. Larie et al., “A 60 GHz 28 nm UTBB FD-SOI CMOS reconfigurable power amplifier with 21% PAE, 18.2 dBm P1dB and 74mW PDC,” in ISSCC15


