A multi-core VCO and a frequency quadrupler for E-Band adaptive modulation links in 55nm BiCMOS

Lorenzo Iotti, Andrea Mazzanti, Francesco Svelto

University of Pavia, Italy
Outline

• E-Band wireless mobile backhaul
• Frequency synthesizer architecture
• Multi-core VCO design
• Frequency quadrupler design
• Measurement results
**E-Band Wireless Backhaul**

- **Small cells** require cheap, high-capacity, short-reach backhaul links
- **mm-Wave E-Band** (71-76/81-86 GHz) allocated for wireless backhaul
- High BTS density motivates **CMOS/BiCMOS backhaul transceiver** development
Frequency Synthesizer Challenges

- Wireless backhaul links employ adaptive modulation (e.g. QPSK to 64QAM) to maximize spectral efficiency according to channel conditions
- Integrated phase noise degrades EVM. Spec depends on modulation order
- 64QAM phase noise spec is very challenging

<table>
<thead>
<tr>
<th>Modulation</th>
<th>L(f) @ 1MHz Spec</th>
</tr>
</thead>
<tbody>
<tr>
<td>QPSK</td>
<td>-90 dBc/Hz</td>
</tr>
<tr>
<td>16 QAM</td>
<td>-96 dBc/Hz</td>
</tr>
<tr>
<td>64 QAM</td>
<td>-102 dBc/Hz</td>
</tr>
</tbody>
</table>
Synthesizer Architecture

- Noise-tunable 20GHz VCO, trades noise and power according to modulation order
- Wideband low-power frequency quadrupler
Noise Scaling in VCOs

\[ L(f) = F \frac{4kTR_T}{A_0^2} \left( \frac{f_0}{2Q\Delta f^2} \right)^2 \approx \frac{4kT}{R_TI_{dc}^2} \left( \frac{f_0}{2Q\Delta f^2} \right)^2 \]

Halving I\text{\textsubscript{dc}} leads to 4x phase noise increase

\[ \downarrow \]

3dB FoM penalty

Halving R\text{\textsubscript{T}} at constant swing leads to 2x noise decrease

\[ \downarrow \]

Constant FoM
Multi-Core VCO

QPSK

Main core

QuadCore_EN

DualCore_EN

Aux core

QuadCore_EN

Aux core

QuadCore_EN

Aux core
Multi-Core VCO

16QAM
-3dB L(f)
Multi-Core VCO

64QAM
-6dB L(f)

Main core

DualCore_EN

QuadCore_EN

Aux core

QuadCore_EN

Aux core

QuadCore_EN

Aux core
Effect of Mismatches

Trade-off on switch size between mismatch tolerance and TR reduction
Effect of Mismatches - Model

\[ \Delta f_{MAX} = \frac{Q}{f_0} \left( \frac{R_C}{R_T} \right) \]

\[ f_{res,1} = f_0 - \Delta f/2 \]
\[ f_{res,2} = f_0 + \Delta f/2 \]

Graphs showing phase shift and oscillation swing reduction vs. \( R_C/R_T \) for different mismatches.
Effect of Mismatches – Phase Noise

At given frequency mismatch, noise penalty rises with \( \frac{R_C}{R_T} \) as a consequence of both swing reduction and phase shift between tank voltages.
Individual Core

[Diagram of an individual core with labels for Core_EN and tank inductor]
• Low-k magnetically-coupled resonators for BW enhancement and SE-to-diff conversion
• High-speed SiGe bipolars for better gain at 80 GHz
• CMOS input stage for direct connection to high-swing VCO
Test Chip

- ST BiCMOS 55nm
- Core area 830x660 μm²
- Vdd 1.2V
- Stand-alone VCO and multiplier also realized on separate chips
Measurement Setup

- **Signal Generator**: 47-70GHz Ext LO
- **4x Amplifier**
- **Buffer** (BUF)
- **Spectrum Analyzer**
  - **15GHz Downconverted Output**
  - **50Ω负载**
VCO Phase Noise

- Phase Noise [dBc/Hz] vs Offset Frequency [Hz]
- Black line: Single Core
- Red line: Quad Core
- Difference: ~ 6 dB
E-Band Phase Noise

Frequency multiplier introduces negligible noise degradation
Measurements with artificially-induced frequency mismatch verify noise degradation model.
Multiplier Output Voltage

Vin = -4 dBV,diff,0pk

- Vout,0-pk [dBV]
- Fout [GHz]
- 27% Fractional BW

- Measurement
- Simulation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pdc</td>
<td>7 mW</td>
</tr>
<tr>
<td>Conv Loss</td>
<td>-8 dB</td>
</tr>
<tr>
<td>Fund Harm Rejection</td>
<td>45 dB</td>
</tr>
<tr>
<td>II Harm Rejection</td>
<td>35 dB</td>
</tr>
</tbody>
</table>
# Performance Summary

<table>
<thead>
<tr>
<th></th>
<th>This (Single)</th>
<th>This (Quad)</th>
<th>Sun RFIC '12</th>
<th>Nakamura JSSC '12</th>
<th>Kang RFIC '11</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Tech</strong></td>
<td>BiCMOS 55nm</td>
<td>BiCMOS 55nm</td>
<td>BiCMOS 130nm</td>
<td>BiCMOS 180nm</td>
<td>BiCMOS 130nm</td>
</tr>
<tr>
<td><strong>Fout [GHz]</strong></td>
<td>84</td>
<td>84</td>
<td>62</td>
<td>52.5</td>
<td>92.7</td>
</tr>
<tr>
<td><strong>Tuning Range</strong></td>
<td>15.8%</td>
<td>15.8%</td>
<td>4.7%</td>
<td>26.5%</td>
<td>8.3%</td>
</tr>
<tr>
<td><strong>L(f) @ 1MHz [dBc/Hz]</strong></td>
<td>-99</td>
<td>-105</td>
<td>-106</td>
<td>-108</td>
<td>-102</td>
</tr>
<tr>
<td><em><em>Eq. L(f)</em> @ 1MHz from 84GHz [dBc/Hz]</em>*</td>
<td>-99</td>
<td>-105</td>
<td>-103</td>
<td>-104</td>
<td>-103</td>
</tr>
<tr>
<td><strong>Vdd [V]</strong></td>
<td>1.2</td>
<td>1.2</td>
<td>3</td>
<td>3</td>
<td>3.3</td>
</tr>
<tr>
<td><strong>Pdc (VCO+Mult) [mW]</strong></td>
<td>20</td>
<td>55</td>
<td>39</td>
<td>132</td>
<td>90</td>
</tr>
<tr>
<td><strong>FoM [dBc/Hz]</strong></td>
<td>-184.5</td>
<td>-186</td>
<td>-185.6</td>
<td>-181.2</td>
<td>-181.8</td>
</tr>
<tr>
<td><strong>FoM_T [dBc/Hz]</strong></td>
<td>-188.5</td>
<td>-190</td>
<td>-179</td>
<td>-189.6</td>
<td>-180.2</td>
</tr>
<tr>
<td><strong>Output</strong></td>
<td>Diff</td>
<td>Diff</td>
<td>SE</td>
<td>SE</td>
<td>Diff</td>
</tr>
</tbody>
</table>

* Eq L(f)=L(f)@1MHz+20log10(84GHz/Fosc)
Conclusions

• A multi-core 20GHz VCO driving a frequency quadrupler was demonstrated in BiCMOS 55nm technology

• The multi-core VCO achieves ultra-low phase noise and 6dB noise scaling at constant FoM

• The frequency quadrupler exploits transformer-coupled resonators to achieve wideband operation with low power

• Effect of mismatches in multi-core VCOs was studied in depth

• Circuits are suitable for E-Band adaptive-modulation links up to 64QAM
This work has been carried on in collaboration with STMicroelectronics, and was partially funded by the European Union 7th Framework Programme (FP7/2007-2013) under grant 619563 (MiWaveS)