A low-power 64-84GHz frequency quadrupler based on transformer-coupled resonators for E-Band backhaul applications

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Outline

• E-Band wireless mobile backhaul
• Frequency synthesizer architecture
• BiCMOS frequency quadrupler design
• Measurement results
Next-Generation Mobile Networks

Massive growth in mobile traffic

5G mobile networks have to meet further growth in mobile service channel capacity

Massive growth in connected devices

Cisco VNI Mobile 2014

Cisco CCS 2013
**Small cells** require cheap, flexible, high-capacity, short-reach backhaul links

**mm-Wave E-Band** (71-76/81-86 GHz) allocated for wireless backhaul

High BTS density motivates **CMOS/BiCMOS backhaul transceiver** development
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Frequency Synthesizer Challenges

- Wireless backhaul links employ **high-order modulation** (64QAM and beyond) to increase channel capacity.
- Integrated phase noise degrades EVM.
- Very severe phase noise requirements for CMOS mm-Wave circuits.

<table>
<thead>
<tr>
<th>Modulation</th>
<th>$L(f) @ 1$MHz Spec</th>
</tr>
</thead>
<tbody>
<tr>
<td>QPSK</td>
<td>-90 dBc/Hz</td>
</tr>
<tr>
<td>16 QAM</td>
<td>-96 dBc/Hz</td>
</tr>
<tr>
<td>64 QAM</td>
<td>-102 dBc/Hz</td>
</tr>
</tbody>
</table>
Synthesizer Architecture

- VCO exploits higher passive Q at 20 GHz for low phase noise
- Wideband, low-power frequency quadrupler required
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Frequency Doublers

- **Push-push doubler**
  - ✔ Very simple
  - ✔ Good efficiency
  - ✔ No phase noise penalty
  - ✗ Single ended output
  - ✗ Limited GBW
Transformer-coupled push-push doubler

- XFMR used as balun for differential output
- IV order load improves GBW
- Low-k XFRM-coupled resonators provide wideband flat Z21
Capacitive Coupling in Balun

- Common-mode current coupled to the output
- Conversion gain drop
- Lower II-harmonic rejection

\[|Ic1| = \omega Cc(Vc1p - Vc1s)\]
\[|Ic2| = \omega Cc(Vc2p - Vc2s)\]
• **GND isolation through bondwires provides high impedance for CM**

• **Dummy coil recollects CM current**

### Simulated quadrupler performance

<table>
<thead>
<tr>
<th></th>
<th>Normal Balun</th>
<th>Isolated Balun</th>
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</thead>
<tbody>
<tr>
<td>Av</td>
<td>-9 dB</td>
<td>-6 dB</td>
</tr>
<tr>
<td>II-Harm Rej</td>
<td>15-25 dB</td>
<td>35 dB</td>
</tr>
</tbody>
</table>
Frequency Quadrupler

- High-speed SiGe bipolar transistors for better gain at 80 GHz
- CMOS input stage for direct connection to high-swing VCO
- Small capacitive banks compensate process mismatches
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Test Chip

- ST BiCMOS 55nm
- Core area 0.08 mm²
- Power 7mW
- Vdd 1V/1.2V
Measurement Setup

Agilent E8257D Signal Generator

15-22GHz Input

Agilent PXA N9030A Spectrum Analyzer

15GHz Downconverted Output

47-70GHz Ext LO

50Ω
Output Voltage

Vin = -4 dBV,diff,0pk

20GHz -3dB BW
Amplitude Mismatch
Phase Noise

\[ PN_{calc} = 4PN_{in} + PN_{DownConversionTone} \]
<table>
<thead>
<tr>
<th></th>
<th>This work</th>
<th>Hung RFIC 2015</th>
<th>Mazzanti ISSCC 2010</th>
<th>Wang ISSCC 2012</th>
<th>Yeh RFIC 2015</th>
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</thead>
<tbody>
<tr>
<td>Mult factor</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>4</td>
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<tr>
<td>Tech</td>
<td>BiCMOS 55nm</td>
<td>SOI 45nm</td>
<td>CMOS 65nm</td>
<td>SiGe 130nm</td>
<td>SiGe 100nm</td>
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<tr>
<td>Outputs</td>
<td>Diff</td>
<td>SE</td>
<td>Diff</td>
<td>SE</td>
<td>SE</td>
</tr>
<tr>
<td>Fout [GHz]</td>
<td>74</td>
<td>100</td>
<td>115</td>
<td>130</td>
<td>50</td>
</tr>
<tr>
<td>Fractional BW</td>
<td>27%</td>
<td>16%</td>
<td>13%</td>
<td>5%</td>
<td>24%</td>
</tr>
<tr>
<td>Vdd [V]</td>
<td>1-1.2</td>
<td>3.6</td>
<td>1</td>
<td>1.6</td>
<td>3.3</td>
</tr>
<tr>
<td>Pdc [mW]</td>
<td>7</td>
<td>240</td>
<td>6</td>
<td>6.5</td>
<td>150</td>
</tr>
<tr>
<td>Gain [dB]</td>
<td>-8</td>
<td>-5</td>
<td>0</td>
<td>0.6*</td>
<td>17</td>
</tr>
<tr>
<td>Aout,0pk</td>
<td>250</td>
<td>950</td>
<td>630</td>
<td>240*</td>
<td>800</td>
</tr>
<tr>
<td>Fund Harm Rejection [dB]</td>
<td>45</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>22</td>
</tr>
<tr>
<td>II Harmonic Rejection [dB]</td>
<td>35</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>22</td>
</tr>
<tr>
<td>Area [mm²]</td>
<td>0.08</td>
<td>N/A</td>
<td>0.015</td>
<td>0.03</td>
<td>0.22</td>
</tr>
</tbody>
</table>

* Including 35mW input buffer
Conclusions

• A 64-84GHz frequency quadrupler with 7mW power consumption was demonstrated in BiCMOS 55nm technology

• It exploits transformer-coupled resonators in interstage and output matching networks for SE-to-differential conversion and GBW enhancement

• CM isolation technique is employed in the baluns, leading to conversion gain and II-harmonic-rejection improvement

• The multiplier is suitable as a building block in a low-phase-noise frequency synthesizer for E-Band backhaul links
Acknowledgement

This work has been carried on in collaboration with STMicroelectronics, and has received funding from the European Union 7th Framework Programme (FP7/2007-2013) under grant agreement 619563 (MiWaveS).