A 45 Gb/s PAM-4 Transmitter Delivering 1.3Vppd Output Swing with 1V supply in 28nm CMOS FDSOI

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Outline

• Motivation

• PAM-4 vs NRZ for 400G

• Proposed TX Architecture
  • High-Swing Voltage Mode Driver
  • High-Speed Serializer

• Measurement Results

• Conclusions
Network Traffic Growth

- 2.8x traffic growth from 2014 to 2019
- Up to 3.5x in busy-hour time
- Traffic from mobile devices will exceed the one from wired devices by 2019

Answer to >25Gb/s interfaces:

- OIF CEI-56G LR/MR/VSR/XSR/USR roadmap
- IEEE 802.3bs 400GbE task force (16x25Gb/s or 8x50Gb/s)
400G Challenges and Opportunities

Challenges
- Gates’ count increase faster than I/O speed
- Power dissipation, rather than technology and routing, mostly limits max I/O density
- Increasing data rate at > 25Gb/s increases link losses and power consumption

Possible solutions
- Aggregate channels (WDM)
- Shorten electrical paths to optics
- Use complex modulation schemes

PAM-4 modulation
- Helps maintain loss budget by decreasing Nyquist frequency
- SNR degradation can be recovered by using FEC
PAM-4 SNR and H Opening

$f_{\text{Nyquist}} = 1/(2\text{Tbit})$
Intrinsic H opening = 1 [UI]
Eye Amplitude = 1

Slight increase in horizontal opening
Noise power is halved, but eye amplitude reduced by 1/3

High TX output amplitude mandatory to keep high SNR
• Ratio of Level Mismatch (RLM) quantifies PAM-4 eye distortion

• $RLM = \frac{3V_{\text{min}}}{V_{\text{ppd}}} = 80\%$ (picture above) yields:
  - 25% reduction in $H$ opening $\rightarrow$ $H$ opening advantage lost
  - 30% reduction in vertical opening @ $10E-6$ with $3mV_{\text{rms}}$ noise

• Standard recommends $RLM > 92\%$
• Theoretical max diff. swing is $\frac{4}{3}(V_{dd}-V_{ov})$
• Linearity limited by tail current sources
• With $V_{dd}=1V$, typically $RLM<85\%$
• Increasing $V_{dd}$ increases linearity but lower efficiency
Voltage-Mode Drivers

- Robust towards non-linear device on-resistance $R_T$
- With $R_E/R_{on}>1/1$, RLM is better than 96%
- However, matching constraints max swing to $V_{DD}$
Swing-Enhanced PAM-4 TX

- Additional currents \( 1/3I_s, 2/3I_s \) injected in the output node
- With \( I_s=3\text{mA}, V_{DD}=1\text{V} \), output swing is raised to 1.3Vppd
- Compared to increasing \( V_{DD} \) to 1.3V, 30% better efficiency
Swing-Enhanced PAM-4 TX

- Driver is transmitting MSB=1 and LSB=1
- Additional current flowing into the load is $I_S = I_{MSB} + I_{LSB}$
Swing-Enhanced PAM-4 TX

- Driver is transmitting MSB=1 and LSB=0
- Additional current flowing into the load is $I_S/3 = I_{MSB} - I_{LSB}$
TX Replica Bias for Levels Calibration

- Small headroom across current sources when delivering large swing → linearity impaired and eye still distorted
- Scaled TX replicas employed for current sources calibration

\[
I_{MSB} - I_{LSB} = \frac{\Delta V}{6R_L}
\]

\[
\alpha (I_{MSB} + I_{LSB}) = \frac{\Delta V}{2R_L}, \alpha < 1
\]
TX Replica Bias for Levels Calibration

Ensures high linearity even with small headroom across current sources:

- Without cal: RLM=83%
- With cal: RLM=97%
• Multiplexers switch either main tap or delayed data to the driver
• Main tap amplitude always automatically maximized
Serializer, Driver and Output Network

- Delay $\Delta T$ to precisely match 2:1 mux timing
- 5 driver slices for output impedance matching
Duty Cycle Correction Circuit

- DCD by process mismatches, supply and temperature variation
- Loop can be disabled and controlled manually
Output Stage and Network

MSB (4 taps)

Tap\(_{-1}\)  Tap\(_0\)  Tap\(_1\)  Tap\(_2\)

LSB (4 taps)

5 TX slices

SST slices
CM driver
SST slices

outP

outN
Output Stage and Network

- 200V MM / 500V CDM, >>2kV HBM ESDs account for 250fF capacitance each
- Parasitic inductor $L_s$ + asymmetric T-coil enhance bandwidth by 150%
Test Chip

- Supply Voltage: 1V
- Data Rate: 45Gb/s
- Power: 120mW
  - Serializer 60mW
  - Replica TX 5mW
  - Bias 5mW
  - Driver 50mW

- 10ML CMOS 28nm FDSOI from STMicroelectronics
- Chips encapsulated in flip-chip BGA packages
Measurement Setup

- Channel profile includes PCB trace, connector and cable losses
- At the frequency of 12GHz, loss is 6dB
Differential Output Impedance

- Output impedance can be set with 4Ω precision
- Output return loss inside IEEE802.3bs mask limit
Output eyes at 10Gb/s

- Data Rate is 10Gb/s
- FIR disabled
- Swing-enhancing currents improve eye amplitude by 30%
- Output levels calibration loop set (V11, V10, V01, V00) ~ (825mV, 610mV, 390mV, 175mV)
Output eyes at 45Gb/s

- Data Rate is 45Gb/s
- FIR is ON and recovers 6dB at Nyquist
- Swing-enhancing currents improve eye amplitude by 28%
- Output levels calibration loop set (V11, V10, V01, V00) ~ (825mV, 610mV, 390mV, 175mV)
Boost vs Coefficients

- Each coefficient provides maximum +/- 6dB boost
- Precision: 5 bits + sign
Eye distortion test 1/2

- Test proposed by CEI-56G and IEEE 802.3bs emerging standards
- \( RLM = 3 \min(V_B - V_A, V_C - V_D, V_D - V_C)/(V_D - V_A) \)
- At 45Gb/s RLM > 0.92 (spec under discussion) for 20 chip samples
• Equalization by using FFE does not impact RLM
## Summary and comparison

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Menolfi ISSCC '05</th>
<th>Nazemi ISSCC '15</th>
<th>Chiang ISSCC '14</th>
<th>Kim ISSCC '15</th>
<th>This Work</th>
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<tbody>
<tr>
<td>CMOS Technology</td>
<td>90nm SOI</td>
<td>28nm</td>
<td>65nm</td>
<td>14nm</td>
<td>28 nm FDSOI</td>
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<td>Driver Topology</td>
<td>CML</td>
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<td>SST</td>
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<tr>
<td>TX-FFE</td>
<td>4-taps</td>
<td>DAC</td>
<td>3-taps</td>
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<td>ESD</td>
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<td>No</td>
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<td>Yes</td>
<td>Yes</td>
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<td>Data-Rate [Gb/s]</td>
<td>25</td>
<td>36</td>
<td>60</td>
<td>40</td>
<td>45</td>
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<tr>
<td>Output Swing $V_{out}$ [Vppd]</td>
<td>0.84$^1$</td>
<td>0.8</td>
<td>0.250</td>
<td>0.9$^3$</td>
<td>1.3</td>
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<td>Vdd [V]</td>
<td>1</td>
<td>1.5</td>
<td>1.2</td>
<td>N/A</td>
<td>1</td>
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<td>Power $P_{DC}$ [mW]</td>
<td>102</td>
<td>84$^2$</td>
<td>205$^2$</td>
<td>167.5$^2$</td>
<td>120</td>
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<td>Power Efficiency ($V_{out}^2/2R)/P_{DC}$ [%]</td>
<td>3.4</td>
<td>3.8</td>
<td>0.15</td>
<td>2.42</td>
<td>7</td>
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<td>mw/Gbps</td>
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<td>2.33</td>
<td>3.4</td>
<td>4.18</td>
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<td>Area [mm$^2$]</td>
<td>0.052</td>
<td>0.05</td>
<td>1.14</td>
<td>0.0279</td>
<td>0.28</td>
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</tbody>
</table>

1 Amplitude from picture. Loss recovered by FFE de-embedded.
2 Not including PLL and clock distribution power.
3 Amplitude from picture. Loss recovered by software CTLE de-embedded.
Conclusions

- High TX pk-to-pk swing and low distortion are key features for high-speed PAM-4 transmitters

- A hybrid, mostly-SST, 45Gb/s PAM-4 transmitter architecture is proposed to deliver 1.3Vppd output swing with 1V supply only

- Calibration through automatic loop ensures low eye distortion, key requirement for next generation PAM-4 transceivers

- Measurements on more than 20 28nm CMOS FDSOI test-chips prove the effectiveness of the proposed TX