A 56Gb/s 300mW Silicon-Photonics Transmitter in 3D-Integrated PIC25G and 55nm BiCMOS Technologies

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Motivation

- Power efficient high speed interconnects are required

Total Data Center Traffic

<table>
<thead>
<tr>
<th>Year</th>
<th>Zettabytes per Year</th>
</tr>
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<tbody>
<tr>
<td>2014</td>
<td>3.4</td>
</tr>
<tr>
<td>2015</td>
<td></td>
</tr>
<tr>
<td>2016</td>
<td></td>
</tr>
<tr>
<td>2017</td>
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<td>2018</td>
<td>10.4</td>
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<td>2019</td>
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Source: Cisco Global Cloud Index, 2014 - 2019
Next generation optical interconnects

100Gb standards/MSA for optical interconnects

- 100Gbase-LR4 (long reach): 4x25Gbps NRZ, 1 fiber (WDM)
- 100Gbase-PSM4 (short reach): 4x25Gbps NRZ, 4 fibers

Moving beyond 100Gbps

- 50Gbps on each fiber
  - (50GBd NRZ or 25GBd PAM4)
- 100Gbps on each fiber
  - (100GBd NRZ or 50GBd PAM4)

50Gbaud signaling
Outline

• Silicon Photonics platform
• Optical modulators
• Modulator architecture and design
  – Transmission line design
  – Equalization implementation
  – Predriver / Driver design
• Experimental results
• Conclusions
Why Silicon Photonics?

• Traditional photonic is limited by high cost and a low level of integration

Silicon Photonics
Integrated TX/RX

Source: F. Boeuf et al. – OFC2015

Silicon Photonics lends itself to low power and low cost optical interconnects with high integration level
Silicon Photonics platform

- 12 inches wafer Silicon Photonics platform (PIC25G)
-Compatible with 3D assembly through Copper Pillars

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E/O package

Picture not to scale
Mach Zehnder Modulators

\[ P_{out} = P_{max} \sin^2 \left( \frac{\Delta \varphi}{2} \right) \]

\[ OMA = P_1 - P_0 \]

\[ ER = \frac{P_1}{P_0} \]
MZMs for Silicon Photonics

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Travelling Wave Architecture

- Travelling Wave MZM is well suited for high speed
  - Simple driving of long structures
  - Low complexity
  - Small EIC area

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Transmission line design

• PIC transmission line needs:
  – Low losses → limit signal attenuation
  – High impedance → low power consumption
  – E/O delay matching → max bandwidth

• Bifilar Tline for high $Z_0$
• HSPM fill ratio optimization
  → E/O delay matching
Transmission line performance

- **Optical edges optimization**
- **Z₀ ≈ 60Ω** has been achieved
  - 3dB/mm attenuation @ 28GHz
  - Critical for 56Gbps operation
Electrical channel response

- Limited bandwidth of Tline
- HSPM sections driven by different electrical channel responses

Careful equalization needed
Modulator driver architecture

- Dual-drive push-pull fully differential configuration
- DC coupling on anode – AC coupling on cathode
- Combination of active and passive equalization
**Input stage**

- Input stage needed for:
  - Input matching
  - Predriving of following stage
- Emitter follower topology
  - Ensure wide output BW
  - Wideband input matching

- Biasing loop to set output $V_{CM}$

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**Figure Description**

- **Input Stage Circuit**:
  - The circuit diagram illustrates the input stage with transistors $M_1$ and $M_2$.
  - $V_{CM}$ and $V_{CCH}$ are voltage sources.
  - The input stage is configured to ensure input matching and wide output bandwidth.

**Graph**

- The graph shows the differential $S11$ plot over frequency, demonstrating the input matching characteristics.
  - The $S11$ values are plotted from 0 to 40 GHz, with a focus on 25 and 35 GHz.
  - The plot indicates good input matching with $S11$ values below -10 dB across the frequency range.
Pre-driver / equalizer

- ECL pairs with shared load
  - High pass path for equalization
  - R/R path for DC gain

- Shunt peaking on load to enlarge bandwidth

- Cascode to avoid SOA issues
Active equalization in pre-driver

\[ k_{EQ} = \frac{I_{EQ}}{I_{DC} + I_{EQ}} \]

\[ k_{EQ} = 0.5 \rightarrow I_{EQ} = I_{DC} \]
Load-coupling passive equalization

\[ k_C = \frac{C_C}{C_L} \quad ; \quad k_R = \frac{2R_{OUT}}{R_L} \]

\[ C_C > C_L \]

\[ R_L > 2R_{OUT} \]

- \( C_L \) avoids DC current flow into \( R_L \)
- Up to 6dB boost achievable
Overall equalization - TF

Overall equalization - TF

Transfer function (dB)

f (Hz)

-16
-14
-12
-10
-8
-6
-4
-2
0

passive only
active only
no equalization
active and passive

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Overall equalization – eye diagrams

- **no EQ**
- **EQ active**
- **EQ passive**
- **EQ active and passive**
**Driver stage**

- Emitter follower to set output levels
- AC coupling for fast current switching
- $V_{REF}/R_E$ biasing from replica to provide stable bias current
Test Chip

- ST PIC25G (PIC)
- ST BiCMOS55 (EIC)
- Cu-Pi 3D mounting
Measurement setup

- Electrical inputs through RF probes
- Optical input/output through optical probes
56Gb/s measurements

1) MZM biased at quadrature
2) MZM biased at increased ER

- PRBS31 pattern
- 2.5dB ER @ quadrature
- 3.5dB ER @ increased ER
- 300mW power dissipation
56Gb/s simulations comparison

- Simulation performed with PRBS9 pattern
- Good agreement with simulations is demonstrated
28Gb/s measurements

1) MZM biased at quadrature
2) MZM biased at increased ER

• PRBS31 pattern
• 3.4dB ER @ quadrature
• 4.6dB ER @ increased ER
• 300mW power dissipation
E/O testboard and package design

• Low cost E/O package design
  – Standard LGA substrate
  – Standard socket interconnections
  – Megtron6 PCB signal layer

![Graph showing frequency vs. S11 and differential insertion loss in dB]

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Packaged sample measurements

- Negligible impact at 40Gbps

- Further equalization needed at 56Gbps
## Comparison – 56Gbps E/O transmitters

<table>
<thead>
<tr>
<th>Item</th>
<th>This work</th>
<th>Denoyer JLT2015</th>
<th>Takemoto OFC2015</th>
<th>Kuchta OFC2013</th>
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<tr>
<td>Wavelength [nm]</td>
<td>1310</td>
<td>1310</td>
<td>1310</td>
<td>850</td>
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<tr>
<td>Data Rate [Gbps]</td>
<td>56</td>
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<td>50</td>
<td>56</td>
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<tr>
<td>Transmitter Architecture</td>
<td>Silicon Photonics MZM</td>
<td>Silicon Photonics MZM</td>
<td>Directly modulated DFB-LD</td>
<td>Directly modulated VCSEL</td>
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<td>Driver Technology</td>
<td>55nm BiCMOS</td>
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<td>Test data pattern</td>
<td>PRBS31</td>
<td>PRBS9</td>
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<td>PRBS7</td>
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<td>Extinction Ratio at quadrature [dB]</td>
<td>2.5</td>
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<td>Driver dissipated power [mW]</td>
<td>300</td>
<td>430</td>
<td>810</td>
<td>682</td>
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</table>
Conclusions

• A 56Gbps silicon photonics MZM-based transmitter in PIC25G and BiCMOS55nm technologies has been presented

• A Twave architecture, together with shunt peaking and passive peaking in the load, has been adopted to overcome transmission line bandwidth limitations

• Efficacy of Silicon Photonics platform together with 3D assembly for 56Gb/s operations has been demonstrated