Serial link interfaces, with emphasis on the challenges of future links

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Network Traffic Growth

- 2.8x traffic growth from 2014 to 2019
- Up to 3.5x in busy-hour time
- Traffic from mobile devices will exceed that from wired devices by 2019

400G: what are the challenges of the next-generation SerDes systems?
Outline

• Motivation
• Trends in the wireline world
• Desiderata and challenges for next-gen links
• Increasing Data Rate: PAM-4 vs NRZ
• High-Speed Equalization: Tunable FIR Filters for MMF
• Conclusions

= hot and promising research topic
Typical Data Center Connections

- Copper backplanes are employed for connections inside the same chassis or among different chassis.
- Optical fibers typically employed for long-reach connections between different buildings or between floors of the same building.
- Depending on speed/cost, Multi-Mode Fibers (MMF) or Single-Mode Fibers (SMF) can be used.
Typical SerDes Architecture
• Per-pin data rate has doubled every four years across a variety of diverse I/O standards
• Scaling helps but now we need more than scaling
• Scaling factor between link power and signaling loss is slightly less than unity
Wish List for Next-Generation 400G

1. Increase link speed without compromising link efficiency [mW/Gpbs]
2. Improve equalizers for longer-reach backplanes
3. Increase the use of MMF, which is more cost effective than SMF
4. Improve boards and package, main source of reflections
5. Improve interface from fiber to chip

Optical Fibers

Backplanes
<table>
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<tr>
<th>Topic</th>
<th>Paper Published</th>
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</table>
| Increasing Data Rate: from NRZ to PAM-4 modulation | • M. Bassi, F. Radice, M. Bruccoleri, S. Erba and A. Mazzanti, "A 45Gb/s PAM-4 transmitter delivering 1.3Vppd output swing with 1V supply in 28nm CMOS FDSOI," ISSCC 2016  
• “A 64Gb/s PAM-4 Transmitter with 4-taps-FFE and 2.26 pJ/bit Energy Efficiency in 28nm CMOS FDSOI”, just accepted at ISSCC 2017 |
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Issues with Increasing Data Rate

- Thanks to technology scaling, gate count increases, but faster than I/O speed and available bumps.
- Power dissipation, rather than technology itself or routing, mostly limits max I/O density.
- Increasing data rate at > 25Gb/s increases link losses and power consumption.
Possible Solutions

PAM-4 modulation vs NRZ
• Helps maintain loss budget by halving Nyquist frequency
• SNR degradation can be recovered by using FEC

PAM-4 SNR and H Opening

56Gb/s, ch. loss is 3dB @ 28GHz

Intrinsic H opening = 1 [UI]

\( f_{\text{Nyquist}} = 1/(2\text{Tbit}) \)

Eye Amplitude = 1

• Slight increase in horizontal opening
• Noise power is halved, but eye amplitude reduced by 1/3

Intrinsic H opening = 1.3 [UI]

\( f_{\text{Nyquist}} = 1/(4\text{Tbit}) \)

Eye Amplitude = 1/3

Delivering high TX amplitude mandatory to preserve high SNR
• Ratio of Level Mismatch (RLM) quantifies PAM-4 eye distortion

• RLM = $3V_{\text{min}}/V_{\text{ppd}} = 80\%$ (picture above) yields:
  o 25% reduction in H opening $\rightarrow$ H opening advantage lost
  o 30% reduction in vertical opening @ 10E-6 with 3mVrms noise

• Standard recommends RLM>92%
PAM-4 Current-Mode Driver

- Theoretical max diff. swing is $4/3(V_{DD}-V_{OV})$
- Linearity limited by tail current sources
- With $V_{DD}=1V$, typically $RLM<85\%$
- Increasing $V_{DD}$ increases linearity but reduces efficiency

![Diagram of PAM-4 Current-Mode Driver](image)
PAM-4 Voltage-Mode Drivers

- Robust towards non-linear device on-resistance $R_T$
- With $R_E/R_{on} > 1/1$, RLM is better than 96%
- However, matching constrains max swing to $V_{DD}$
Proposed Swing-Enhanced PAM-4 TX

- Additional currents \((1/3I_s, 2/3I_s)\) injected in the output node
- With \(I_s=3\text{mA}, V_{DD}=1\text{V}\), output swing is raised to 1.3Vppd
- Compared to increasing \(V_{DD}\) to 1.3V, 30% better efficiency

[Joy et al, ISSCC ‘11]
Proposed Swing-Enhanced PAM-4 TX

- Driver is transmitting MSB=1 and LSB=1
- Additional current flowing into the load is $I_S = I_{MSB} + I_{LSB}$
Proposed Swing-Enhanced PAM-4 TX

• Driver is transmitting MSB=1 and LSB=0

• Additional current flowing into the load is \( I_{S/3} = I_{MSB} - I_{LSB} \)
**TX Replica Bias for Levels Calibration**

- Small headroom across current sources when delivering large swing → linearity impaired and eye still distorted
- Scaled TX replicas employed for calibration of current sources

\[
I_{MSB} - I_{LSB} = \frac{\Delta V}{6R_L}
\]

\[
\alpha(I_{MSB} + I_{LSB}) = \frac{\Delta V}{2R_L}, \alpha < 1
\]
TX Replica Bias for Levels Calibration

Ensures high linearity even with small headroom across current sources:

- Without cal: RLM=83%
- With cal: RLM=97%
TX Driver with FFE

- Each tap made of 6 slices to implement FFE coefficients
- Multiplexers switch either main tap stream or delayed data to the driver
Test Chip

10ML CMOS 28nm FDSOI from STMicroelectronics

Chips encapsulated in flip-chip BGA packages

- Supply Voltage: 1V
- Data Rate: 45Gb/s
- Power: 120mW
  - Serializer 60mW
  - Replica TX 5mW
  - Bias 5mW
  - Driver 50mW
Measurement Setup

- Channel profile includes PCB trace, connector and cable losses
- At the frequency of 12GHz, loss is 6dB
Output Eyes at 10Gb/s

- Data Rate is 10Gb/s
- FFE disabled
- Swing-enhancing currents improve eye amplitude by 30%
- Output levels calibration loop set (V11, V10, V01, V00) ~ (825mV, 610mV, 390mV, 175mV)
- Data Rate is 45Gb/s
- FFE is ON and recovers 6dB at Nyquist
- Swing-enhancing currents improve eye amplitude by 28%
- Output levels calibration loop set (V11, V10, V01, V00) ~ (825mV, 610mV, 390mV, 175mV)
Eye distortion test

- Test proposed by CEI-56G and IEEE 802.3bs emerging standards
- \[ RLM = 3 \min(V_B - V_A, V_C - V_D, V_D - V_C)/(V_D - V_A) \]
- At 45Gb/s \( RLM > 0.92 \) (spec under discussion) for 20 chip samples
# Summary and comparison

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Menolfi ISSCC '05</th>
<th>Nazemi ISSCC '15</th>
<th>Chiang ISSCC '14</th>
<th>Kim ISSCC '15</th>
<th>This Work</th>
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<tbody>
<tr>
<td>CMOS Technology</td>
<td>90nm SOI</td>
<td>28nm</td>
<td>65nm</td>
<td>14nm</td>
<td>28 nm FDSOI</td>
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<td>Driver Topology</td>
<td>CML</td>
<td>CML</td>
<td>CML</td>
<td>SST</td>
<td>SST</td>
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<tr>
<td>TX-FFE</td>
<td>4-taps</td>
<td>DAC</td>
<td>3-taps</td>
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<td>4-taps</td>
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<td>ESD</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>Data-Rate [Gb/s]</td>
<td>25</td>
<td>36</td>
<td>60</td>
<td>40</td>
<td>45</td>
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<tr>
<td>Output Swing Without FFE [Vppd]</td>
<td>0.84&lt;sup&gt;1&lt;/sup&gt;</td>
<td>0.8</td>
<td>0.250</td>
<td>0.93&lt;sup&gt;3&lt;/sup&gt;</td>
<td>1.3</td>
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<tr>
<td>Vdd [V]</td>
<td>1</td>
<td>1.5</td>
<td>1.2</td>
<td>N/A</td>
<td>1</td>
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<tr>
<td>Power $P_{DC}$ [mW]</td>
<td>102</td>
<td>84&lt;sup&gt;2&lt;/sup&gt;</td>
<td>205&lt;sup&gt;2&lt;/sup&gt;</td>
<td>167.5&lt;sup&gt;2&lt;/sup&gt;</td>
<td>120</td>
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<tr>
<td>Power Efficiency ($V_{out}^2/2R)/P_{DC}$ [%]</td>
<td>3.4</td>
<td>3.8</td>
<td>0.15</td>
<td>2.42</td>
<td>7</td>
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<tr>
<td>mw/Gbps</td>
<td>4</td>
<td>2.33</td>
<td>3.4</td>
<td>4.18</td>
<td>2.6</td>
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<tr>
<td>Area [mm&lt;sup&gt;2&lt;/sup&gt;]</td>
<td>0.052</td>
<td>0.05</td>
<td>1.14</td>
<td>0.0279</td>
<td>0.28</td>
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</tbody>
</table>

<sup>1</sup> Amplitude from picture. Loss recovered by software CTLE de-embedded.

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Dispersion in Multi-Mode Fibers

- Large fiber core size enables propagation of several modes
- Different speed leads to different time of arrival and pulse broadening
- 3 different pulses proposed in IEEE802.3aq to represent channel response
Electronic Dispersion Compensation

- Flexible DSP-based EDCs proposed for 10GBASE-LRM
- Analog EDC more efficient at Data-Rate > 10Gb/s
- FIR Equalizer is the most critical block:
  1. Boost at Nyquist frequency must be tunable from 10 to 25Gb/s
  2. Must be low noise and highly linear to sustain high amplitude levels to preserve SNR
  3. Must be area-efficient to be fitted in between two bumps
**FIR Equalizer Block Diagram**

**Td Implementation options:**
- Continuous-time LC-base delay lines, but large area and low tuning range
- Discrete-Time sampled delay lines, but clock generation and distribution issues with

**Proposed FIR:**
- Compact 7 TAP active tunable delay
- 10 to 25Gb/s with scalable power dissipation
Analog Delay: First Order All Pass Filter

- Bandwidth independent from delay
- Variable delay by tuning the pole time constant
- Group delay roll-off is not an issue

\[ y(s) = \frac{2}{1+s\tau} - 1 = \frac{1-s\tau}{1+s\tau} \]

G. D. = \( -\frac{\partial \varphi}{\partial \omega} = \frac{2\tau}{1 + (\omega\tau)^2} \)
Analog Delay: Circuit Realization

- $g_{m1}$ and the RC load form the programmable lowpass filter
- $g_{m2}$ and $g_{m3}$ are used to subtract input signals
- $g_{m2}$ has maximum input swing ($2V_{in}$) and limits linearity
Analog Delay: Circuit Realization

- Maximum now on $g_{m1}$ limited to $V_{in}$
- 1dB C.P ~220mV 0-pk diff (~ +6dB)
- Programmable group delay from 30 to 75ps
- Cell bandwidth from 14GHz to 25GHz
Taps: Programmable Transconductors

\[ I_{\text{OUT}} = (2N - 63) \sqrt{4K_n 'I_{\text{BIAS}} \frac{W_{M_{n1}}}{L_{M_{n1}}}} \]

- Resolution: 6BIT thermometric
- Very large capacitance (~250fF) on the summing node
- Transimpedance amplifier used for summing output currents
Trans-Impedance Amplifier

- Common source topology with peaking inductors
- Programmable bandwidth, gain, and dissipation
- Low MOS gain ($g_m/g_{ds} \sim 5$) impair performances
- Negative $R$ to cancel output conductances
Test Chip

- 10ML CMOS 28nm LP from STMicroelectronics
- Core area: 0.085mm$^2$
- Supply Voltage: 1V
- Data rate: 10 to 25Gb/s
- Power: 55 to 90mW
  - 5.5 to 9mW Delay
  - 10 to 25mW TIA
  - 7x1.5mW Multipliers
MMF Link Emulation Setup

- First chip emulates MMF pulse response
- A second chip (DUT) performs equalization
- Output connected to a sampling scope
- Coefficients adapted with a PC running a MMSE algorithm

Pulse responses spread over 4-5 symbol periods
25Gbps Eye Diagram Measurement Results

- Td=3/4 Tbit (30ps)
- H. and V. openings better than 43% and 57%
- ~100mV vertical amplitude
- Integrated output noise <4mV_{rms}
“Postcursor” channel has a fairly regular low-pass shape

Can be equalized with a simple high-pass response

Adjusting Td gives minor performance improvement
Eye Diagram at 10Gbps

- “Split-A” channel has an in-band notch
- Setting a larger Td shifts the FIR equalizing capability to lower frequency
- Increasing Td improves H. opening from 48% to 69%
## Summary and comparison

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Tech.</th>
<th>Data Rate [Gb/s]</th>
<th># Taps</th>
<th>Total Delay [ps]</th>
<th>Power [mW]</th>
<th>Power / (DataRate•TotalDelay) [mW]</th>
<th>Core Area* [mm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wu JSSC 2003</td>
<td>180n SiGe</td>
<td>10</td>
<td>7</td>
<td>300</td>
<td>40</td>
<td>13.3</td>
<td>1.9</td>
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<tr>
<td>Reynolds ISSCC 2005</td>
<td>130n CMOS</td>
<td>10</td>
<td>7</td>
<td>450</td>
<td>325</td>
<td>72.2</td>
<td>3.8</td>
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<td>Sewter JSSC 2006</td>
<td>90n CMOS</td>
<td>24 - 30</td>
<td>3</td>
<td>70</td>
<td>25</td>
<td>14.8 - 11.9</td>
<td>0.3</td>
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<td>Sewter JSSC 2006</td>
<td>180n CMOS</td>
<td>30 - 40</td>
<td>3</td>
<td>50</td>
<td>70</td>
<td>46.6 - 35</td>
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<td>Momtaz JSSC 2010</td>
<td>65n CMOS</td>
<td>40</td>
<td>7</td>
<td>75</td>
<td>65</td>
<td>21.6</td>
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<tr>
<td>This Work</td>
<td>28n CMOS</td>
<td>10 - 25</td>
<td>7</td>
<td>450 - 180</td>
<td>55 - 90</td>
<td>12.2 - 20</td>
<td>0.085</td>
</tr>
</tbody>
</table>

* Estimated from chip micrograph
Conclusions

• Evolution of serial links is fast and challenging - and several technologies still need to converge to achieve 400Gb/s operation

Key research topics are:
• PAM-4 modulation to decrease Nyquist frequency
  • How to deliver efficient high TX amplitude with CMOS supply
  • How to make a reconfigurable NRZ/PAM-4 TX
  • How to get high linearity for TX and RX chain
  • How to deal with increased number of DFE samplers
• Analog equalizers: low area, high linearity (key for PAM-4), delay tunability, LMS-friendly