A 64Gb/s PAM-4 Transmitter with 4-Tap FFE and 2.26pJ/b Energy Efficiency in 28nm CMOS FDSOI

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Outline

• Motivation

• Proposed TX Architecture
  • Reconfigurable FFE
  • Output Driver
  • High-Speed Serializer
  • Clock Generation

• Measurement Results

• Conclusions
Network Traffic: Growth and Challenges

Challenges

- Gate count increases faster than I/O speed
- Power dissipation, rather than technology and routing, mostly limits max I/O density
- Increasing data rate at > 25Gb/s increases link losses and power consumption

PAM-4 Modulation

- Helps maintain loss budget by decreasing Nyquist frequency
- SNR degradation can be recovered by using FEC

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High-Speed PAM-4/NRZ TX Design

PAM-4

- High output amplitude and linearity – to preserve SNR and H/V opening

PAM-4

- Very high bandwidth – to speed-up non-adjacent level transitions

PAM-4/NRZ

- Precise and reliable serialization with low power

PAM-4/NRZ

- Reconfigurable FFE – to be compliant with several standards

PAM-4/NRZ

- PAM-4/NRZ high/low speed modes – for auto-negotiation and substitution of legacy components

Challenges
• Shift-registers delay 8bit bundles and generate five $C_{[-2:2]}$ FFE data-streams
• MUXs $M_M$ and $M_L$ enable $C_{[-2:2]}$ selection
• In PAM-4 mode, up to 4 FFE taps
• In NRZ mode, 40b LSB/MSB data is merged, but $M_M$ and $M_L$ can still be operated independently to provide up to 5 FFE taps
• Output driver is composed of 72 elements
• 24 driver elements are driven by LSB data, 48 by MSB data
• Dedicated voltage supply $V_{dd,DR}=1.2V$
TX Block Diagram

- PLL generates 2-8GHz clock signal
- High precision I/Q signals generator feeds the 40:1 serializer
Reconfigurable TX FFE

- At Full-Speed, it provides up to 4 FFE tap in PAM-4 mode and 5 tap in NRZ mode, meeting OIF CEI 56Gb/s MR and 28Gb/s KP4 standards

- At Half-Speed, data is oversampled and \([C_{-2}, C_2]\) are mapped as 1-Pre/Post cursor, respectively, meeting 10Gb/s KR10 and 8.5Gb/s PCI Exp-3

- At Quarter-Speed, \(C_2\) is mapped as 1-Postcursor while \(C_{-2:1}\) are all set to the Main cursor. This configurations is compliant with 2.5Gb/s PCI-Exp1

<table>
<thead>
<tr>
<th>Coefficients Minimum Normalized Amplitude</th>
<th>2-PRE</th>
<th>1-PRE</th>
<th>MAIN</th>
<th>1-POST</th>
<th>2-POST</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PAM-4 FS</strong></td>
<td>-3/24</td>
<td>12/24</td>
<td>-9/24</td>
<td>-9/24</td>
<td></td>
</tr>
<tr>
<td><strong>NRZ FS</strong></td>
<td>-21/72</td>
<td>-21/72</td>
<td>36/72</td>
<td>-36/72</td>
<td>-36/72</td>
</tr>
<tr>
<td><strong>NRZ HS</strong></td>
<td>-21/72</td>
<td>-21/72</td>
<td>36/72</td>
<td>-36/72</td>
<td>-36/72</td>
</tr>
<tr>
<td><strong>NRZ QS</strong></td>
<td></td>
<td></td>
<td>45/72</td>
<td>-27/72</td>
<td></td>
</tr>
</tbody>
</table>
State-of-the-art PAM-4 Output Drivers

- Hybrid voltage/current driver
- Very good linearity and high output amplitude with 1V supply
- Bandwidth limited by increased load
- Low FFE programmability

- Pure current mode driver
- Simple implementation, high bandwidth
- Two supply domain and need of level shifter operating at output symbol rate
- High FFE programmability

[Bassi et al., ISSCC 2016, JSSC 2017]

[Nazemi et al., ISSCC 2016]
Proposed Current Mode Driver

- $I_{N}$ and $I_{P}$ CMOS-level input data streams from serializer
- Gate voltages of $M_{C1,2}$ current sources are constant, set by replica bias based on desired output swing $V_{\text{ref}}$
- When output node is high, $M_{C1,2}$ source is pulled to $V_{dd,\text{CMOS}}$, relaxing reliability constraints and allowing the use of thin oxide devices

⇒ High output swing with good linearity and large bandwidth
Output Network

- 200V MM / 500V CDM, >>2kV HBM ESDs
- Driver capacitance is comparable with ESD capacitance
- Double T-coil network enhances bandwidth by 1.5 and improves impedance matching at high frequency
High-Speed Serializer Architectures

Half-rate architecture

- $t_{\text{BIT}} > t_{\text{Setup}} + t_{\text{MUX}} + t_{\text{DIV}} - t_D$
- Low $C_{\text{PAR}}$ load of half-rate architecture leads to very fast commutations

Quarter-rate architecture

- $t_{\text{BIT}} > t_{\text{Setup}} + t_{\text{MUX}} - t_{\text{PULSE}}$
- Higher $C_{\text{PAR}}$ load of quarter-rate architecture leads to increased ISI

- Propagating clock forward relaxes serializer timing constraints
- Low load highly desirable to limit ISI
Proposed MUX Architecture

- Quarter-rate architecture to enhance speed and lower ISI
- Local X2 clock multiplier to save power
- Forward propagated delay implemented with X2 allows relaxed timing constraints:
  - \( t_{\text{BIT}} > t_{\text{Setup}} + t_{\text{MUX}} - t_{\text{MULT}} \)
Proposed MUX Architecture

- MUX 4:2 based on pass-gate to save power and guarantee $t_{MUX} > t_{MULT}$ to respect hold-time constraints
- NAND-based frequency doubler generates half rate clock for the last 2:1 MUX
- At 32 Gsym/s the Pk-Pk jitter on output node is reduce by 1.3 compared to a traditional direct 4:1 MUX
Effects of I/Q Mismatches

- I/Q mismatches on quarter-rate clocks creates DCD on half-rate clock
- I/Q phase difference must be lower than 1.4°
Effects of I/Q Duty-Cycle Distortion

- DCD on quarter-rate I/Q clocks translates to DCD on half-rate clocks with period of 4UI

✓ Generation of precise I/Q quarter-rate clocks is key, especially at high-speed
Clock Generation Tree

- Integer-N type PLL with two VCOs and output divider to generate 2-8GHz master clock
- Injection-Locking Ring Oscillator provides high-accuracy 8 phases against PVTs
- Phase rotators interpolate 8 $\pi/4$-spaced phases to improve DNL and INL
- Quarter-rate clocks fed to serializer after DCC circuit
**Injection Locked Ring Oscillator**

A phase detector based on passive mixers measures the quadrature error and continuously tunes the oscillator Vtune for fine phase correction.

Concurrently, a window comparator monitors Vtune and drives digital coarse calibration in background.

The quadrature phase error is kept lower than 1.5° when supply and temperature variations are between [0.9V, 1.2V] and [-40°C, 120°C]
Phase Rotator

- Phase Rotators consist of four slices driven by the ILRO outputs
- Each slice consists of 32 differential pair thermometric weighted to reduce switching glitches and guarantee the monotonicity of the output phase
- At 11GHz, the maximum DNL and INL are 0.5 and 1 LSB, respectively
DCD Correction Circuit

- PMOS and NMOS switches operates independently
- Two 7 bit thermometric code to avoid glitches and guarantee the monotonicity of the correction
- DCD correction circuit capability equal to ±1.5% at 8GHz
Chip Photo and Power Break-Down

- Power Consumption: 145mW @ 64Gb/s
- $V_{dd,CMOS} = 1V$
- $V_{dd,DR} = 1.2V$

- 10ML CMOS 28nm FDSOI CMOS from STMicroelectronics
- Chips encapsulated in flip-chip BGA packages
Measurement Setup

- Package and trace board loss at 16GHz is 2.5dB
- Connectors and cable add about two more dB of loss
- Total loss at 16GHz equal to 4.5dB
Output Eyes at 28/56 Gb/s

- FIR setting:
  \([C_{-1} \ C_0 \ C_1]=[-1/24 \ 18/24 \ -3/24]\)
- Vertical opening: 0.73V
- Horizontal opening: 0.84UI

- FIR setting:
  \([C_{-1} \ C_0 \ C_1]=[-1/24 \ 18/24 \ -3/24]\)
- Vertical opening: 0.18V
- Horizontal opening: 0.48UI
Output Eyes at 32/64 Gb/s

PRBS-9 @ 32Gb/s

- FIR setting: \([C_{-1} \ C_0 \ C_1]=-1/24\ 18/24\ -3/24\]
- Vertical opening: 0.6V
- Horizontal opening: 0.75UI

QPRBS-13 @ 64Gb/s

- FIR setting: \([C_{-1} \ C_0 \ C_1]=-1/24\ 18/24\ -3/24\]
- Vertical opening: 0.14V
- Horizontal opening: 0.36UI
S22 and PLL Phase Noise

- Return loss better than the mask limit with margin
- Jitter of the clock is estimated by integrating phase noise starting from 500kHz offset
- The random jitter integrated up to 8GHz is 290fs
## Comparison with State of Art

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Kim ISSCC 2015</th>
<th>Lee JSSC 2016</th>
<th>Nazemi ISSCC 2015</th>
<th>Gopalakrishnan ISSCC 2016</th>
<th>Bassi ISSCC 2016</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>14nm FinFET</td>
<td>65nm</td>
<td>28nm</td>
<td>28nm</td>
<td>28nm FDSOI</td>
<td>28nm FDSOI</td>
</tr>
<tr>
<td>Architecture</td>
<td>quarter-rate</td>
<td>half-rate</td>
<td>half-rate</td>
<td>half-rate</td>
<td>half-rate</td>
<td>quarter-rate</td>
</tr>
<tr>
<td>Data Rate [Gb/s]</td>
<td>16-40</td>
<td>60</td>
<td>36</td>
<td>50</td>
<td>45</td>
<td>64</td>
</tr>
<tr>
<td>FFE</td>
<td>NO FFE PAM4</td>
<td>3-taps</td>
<td>DAC</td>
<td>3-taps</td>
<td>4-taps</td>
<td>4-taps</td>
</tr>
<tr>
<td>Power* [mW]</td>
<td>167</td>
<td>205</td>
<td>84</td>
<td>-</td>
<td>120</td>
<td>145** @ 64Gb/s</td>
</tr>
<tr>
<td>Output Swing w/o FFE [Vppd]</td>
<td>0.9</td>
<td>0.25</td>
<td>0.8</td>
<td>-</td>
<td>-</td>
<td>1.2</td>
</tr>
<tr>
<td>RLM [%]</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>&gt;94</td>
<td>94</td>
</tr>
<tr>
<td>Random Jitter [ps$_{rms}$]</td>
<td>0.380 (from scope)</td>
<td>0.508 (from 100kHz to 1GHz, PLL only)</td>
<td>0.1 (from 100kHz to 10MHz, PLL only)</td>
<td>-</td>
<td>0.291 (from 500kHz to 8GHz, Clock Pattern)</td>
<td></td>
</tr>
<tr>
<td>TX pJ/bit</td>
<td>4.1</td>
<td>3.4</td>
<td>2.33</td>
<td>-</td>
<td>2.6</td>
<td>2.26</td>
</tr>
</tbody>
</table>

* Without PLL and Multiphase Clock Generation.
** Including clock distribution buffers.
Conclusions

- Delivering high TX amplitude while preserving linearity and large bandwidth is key for high-speed PAM-4 transmitters

- A new output driver allows high swing and good linearity with increased supply while still employing thin-oxide devices operated reliably

- A smart FFE structure is proposed for back-compatibility with legacy standards

- Measurements test chips realized in 28nm CMOS FDSOI technology by STMicroelectronics prove the effectiveness of the proposed TX
Acknowledgement

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