A 4.9pJ/b 16-to-64Gb/s PAM-4 VSR Transceiver in 28nm CMOS FDSOI

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Outline

• Motivation

• RX Architecture
  • Analog Front-End
  • Sampling Stage

• TX Architecture
  • Current & Voltage-Mode Drivers

• Measurement Results

• Conclusions
Network Traffic: Growth and Challenges

Challenges
- Increasing of data traffic drives wireline systems development
- Unwanted costly infrastructures upgrade
- Increasing data rate at >25Gb/s increases link losses and power consumption

PAM-4 Modulation
- Half bandwidth requirement for given transfer rate
- SNR degradation can be recovered by using FEC
High-Speed PAM-4 Design

Challenges

- High output amplitude and linearity – to preserve SNR and H/V eye opening
- Very high bandwidth – to speed-up non-adjacent level transitions
- Compliance of legacy components
- Very high sensitivity of the samplers due to vertical eye opening reduction
- Different data-rates and supporting of NRZ signaling
Standards

Different standards have been proposed for PAM-4 systems according to channel loss.

- The targets are links up to 15 - 20dB loss @ 28GHz

- Compact and low power analog PAM-4 transceiver without DFE
- Quarter rate clocking
- Reconfigurable PAM-4 / NRZ
- Clock recovery
- Digital calibrations engine
- Internal eye monitor and BER checker
Clock Generation Tree

- Integer-N PLL with two VCOs and output divider generates 2-8GHz master clock
- Injection-Locking Ring Oscillator provides high-accuracy 8 phases against PVTs
- CML phase rotators interpolate 8 π/4-spaced phases to generate 128 output phases with DNL/INL < 1 LSB
- Duty cycle correction circuit on each path
• T-coil Input Network
• Two VGA stages
• Three stages analog equalizer
• Offset cancellation circuit
VGA Known Solutions (1/2)

Differential pair with resistive degeneration

**Advantages:**
- Good linearity
- Simple implementation
- Low input capacitance

**Disadvantages:**
- Parasitic boost
- Bandwidth variation
- Difficult to achieve linear steps

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[ Peng et al., ISSCC 2017 ]
[ Cui et al., ISSCC 2016 ]
VGA Known Solutions (2/2)

Differential pair in Gilbert Cell Configuration

Advantages:
- Linear steps
- Constant bandwidth
- No parasitic boost

Disadvantages:
- Poor linearity
- High input/output caps
- Power consumption

[Mammei et al., JSSC 2014]
[Liao et al., ISSCC 2006]
A mixed solution aims to take the advantages of the two previous solutions mitigating the drawbacks.
VGA Calibration

Phase 1

- The task of the VGA2 is to provide a proper signal amplitude to the sampling stages.
- The VGA2 has to compensate for CTLE gain variation according to its setting.
- A known amplitude signal is provided at the inputs of the CTLE in order to allow VGA2 calibration.

Known Amplitude

VGA1 → CTLE → VGA2

LPBK

From TX

Expected Amplitude
VGA Calibration

- The input signal amplitude is unknown and can vary in the range from 400mV to 1200mV pp-diff
- The task of the VGA1 is to provide a proper signal amplitude to the CTLE
- The VGA1 gains are swept until the desired value is reached
Different effects contribute to channel loss at different frequencies.

The CTLE is made of three stages to better fit losses due to the different contributions.
CTLE Schematic

- Low and mid frequency: transfer function shaped through $R_2$ & $C_s$
- High frequency: boost set by a feedback stage yielding minimal impact at mid frequency and compatibility with LMS adaptation

\[
H_{HF}(s) = -\frac{g_{m5}R_3\left(1 - \frac{s}{\omega_1}\right)}{\left(1 - \frac{s}{\omega_1}\right)\left(1 - \frac{s}{\omega_2}\right)}
\]

\[
\omega_1 \approx \omega_t \left(1 - \frac{\omega_p}{\omega_p - \omega_t}G_{LOOP}\right)
\]

\[
\omega_2 \approx \omega_p \left(1 - \frac{\omega_t}{\omega_p - \omega_t}G_{LOOP}\right)
\]
Effect of the MID Frequency Stage

Aimed at compensating for dielectric losses in the range ~1-10GHz
Effect of the LOW Frequency Stage

Accurate compensation of the skin loss and contribution to improve channel inversion in the transitions area

Accurate compensation of the skin loss and contribution to improve channel inversion in the transitions area
Effect of the HIGH Frequency Stage

Fine channel inversion near Nyquist frequency

Gain [dB]

1E+8 1E+9 1E+10

Frequency [Hz]

Gain [dB]

ANALOG FRONT-END

MID Freq
MID Freq

HIGH Freq

LOW Freq

CTLE

VGA1

VGA2

0.42UI
39mV

0.45UI
40mV

200mV
Sampling Stage (1/2)

Circuit implementation of sampling chain blocks
Sampling Stage (2/2)

- The absence of the DFE allows the introduction of a Track and Hold circuit
- The valid sampling window is doubled
• Reconfigurable PAM-4 / NRZ Quarter Rate architecture
• FIR provides 4 taps PAM-4 and 5 taps NRZ
• MSB and LSB streams are mixed at the driver output
Current Mode Driver

When output node is high, $M_{C1,2}$ sources are pulled to $V_{dd,CMOS}$ relaxing reliability constraints and allowing the use of thin oxide devices and dedicated supply

High output swing with good linearity

10-90\% rise/fall time limited by

$$\tau_{CM} = 25\Omega \cdot (C_{DR} + C_{ESD}) \cdot 2.2$$

ESD Target: 200V MM / 500V CDM, >2kV HBM
Voltage Mode Driver

- The capacitance $C_{DR}$ is charged/discharged with the low $r_{on}$.
- Dominant pole of voltage mode driver is set by $C_{ESD}$ only.

$$\tau_{VM} = 25\Omega \cdot C_{ESD} \cdot 2.2 \approx 0.5 \cdot \tau_{CM}$$
Voltage Mode Driver

- Bandwidth enhancement using T-Coils network
- Output impedance calibrated with resistors in series with Vdd/Gnd. Capacitors introduce a zero, further increasing speed
Chip Photo and Power Break-Down

- 10ML 28nm FDSOI CMOS from STMicroelectronics
- Chips encapsulated in flip-chip BGA package
- Overall power consumption @ 64Gb/s is 315mW
Driver S22

- Return loss better than the mask limit with margin for both Voltage and Current Mode drivers.

Graph showing S22 parameters with frequency on the x-axis and S22 [dB] on the y-axis.
VM vs CM NRZ

- PRBS-13
- FIR setting: $[C_{-1} C_0 C_1]=[-1/24 18/24 -3/24]$

NRZ: VM & CM feature similar performance
VM vs CM PAM-4

- QPRBS-13
- FIR setting: \([C_{-1} \ C_0 \ C_1] = [-1/24 \ 18/24 \ -3/24]\)

PAM-4: Higher speed of the VM driver yields remarkable performance improvement against CM
TX+RX Measurement Setup

- Overall BGA-to-BGA loss is 16.8dB @ 16GHz
- GUI implemented to monitor and control device settings and calibration
RX NRZ Measurement

- Signal quality measured through eye-opening BER contours and bathtub curve
- At 32Gb/s, the horizontal eye opening at BER=10^{-12} is 0.35UI
• At 64Gb/s PAM-4 the horizontal opening is 0.19UI at BER=10^{-6}
• Bathtub is still open at BER=10^{-12}
• Marginal degradation due to crosstalk with two links on
Jitter Tolerance

![Graph showing jitter tolerance tests, performed at maximum speed, meet CEI-56G-VSR mask](image)

Jitter tolerance tests, performed at maximum speed, meet CEI-56G-VSR mask
### TX summary and comparison

<table>
<thead>
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<tbody>
<tr>
<td>Technology</td>
<td>14nm CMOS</td>
<td>16nm FinFET</td>
<td>40nm CMOS</td>
<td>28nm FDSOI</td>
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<tr>
<td>Data Rate [Gb/s]</td>
<td>56</td>
<td>56</td>
<td>56</td>
<td>64</td>
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<tr>
<td>Driver Voltage</td>
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<td></td>
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<td>Voltage</td>
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<tr>
<td>Driver Current</td>
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<td></td>
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<tr>
<td>Swing [V]</td>
<td>0.9</td>
<td>1.2</td>
<td>N/A</td>
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<tr>
<td>FFE</td>
<td>3-tap</td>
<td>3-tap</td>
<td>3-tap</td>
<td>4-tap</td>
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<tr>
<td>RLM [%]</td>
<td>N/A</td>
<td>97</td>
<td>N/A</td>
<td>&gt;94</td>
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<tr>
<td>Area [mm²]</td>
<td>0.035</td>
<td>1.4 (TX+RX)</td>
<td>0.8</td>
<td>0.12</td>
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<td>Supply [V]</td>
<td>0.95</td>
<td>0.9/1.2</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Power [mW]</td>
<td>101</td>
<td>140</td>
<td>200</td>
<td>135</td>
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<tr>
<td>Efficiency [pJ/bit]</td>
<td>1.8</td>
<td>2.18</td>
<td>3.57</td>
<td>2.1</td>
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## RX comparison with State of the Art

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<td>Data rate [Gb/s]</td>
<td>56</td>
<td>56</td>
<td>56</td>
<td>64</td>
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<tr>
<td>Loss [dB]</td>
<td>31</td>
<td>10</td>
<td>24</td>
<td>16.8</td>
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<tr>
<td>Equalization</td>
<td>TX FIR CTLE</td>
<td>TX FIR CTLE</td>
<td>TX FIR CTLE</td>
<td>TX FIR CTLE</td>
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<tr>
<td></td>
<td>24-tap FFE (ADC based)</td>
<td>10-tap DFE</td>
<td>3-tap DFE</td>
<td></td>
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<tr>
<td>Min BER</td>
<td>~1E-8</td>
<td>~ 1E-12</td>
<td>&lt; 1E-12</td>
<td>~ 1E-12</td>
</tr>
<tr>
<td>H @10^-6 BER [UI]</td>
<td>0.15</td>
<td>0.2</td>
<td>0.36</td>
<td>0.19</td>
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<tr>
<td>Area [mm²]</td>
<td>1.4 (TX+RX)</td>
<td>0.36</td>
<td>1.26</td>
<td>0.32</td>
</tr>
<tr>
<td>Supply [V]</td>
<td>0.9/1.2</td>
<td>0.9/1.2</td>
<td>1/1.5</td>
<td>1</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>370*</td>
<td>230</td>
<td>382</td>
<td>180</td>
</tr>
<tr>
<td>Efficiency [pJ/bit]</td>
<td>6.6</td>
<td>4.1</td>
<td>6.8</td>
<td>2.8</td>
</tr>
</tbody>
</table>

*DSP power not included

TX+RX energy efficiency is 4.9pJ/bit. Accounting the 60mW power for clock generation, shared between eight transceivers, the total link energy rises to 5.02pJ/bit only.
Conclusions

A PAM-4 transceiver operating up to 64Gb/s has been presented:

- RX AFE comprises two VGAs and a 3-stage equalizer chain achieving good channel matching. Quarter-rate samplers with track and hold relax comparators speed and meet performance at low power

- CM and VM drivers have been compared in the TX. A modified VM topology allows good linearity and high bandwidth, yielding remarkable improvement in PAM-4 eye opening

- Measurements of test chips in 28nm CMOS FDSOI prove compliance with CEI-56G-VSR at the highest energy efficiency
Acknowledgements

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