

DOTTORATO DI RICERCA IN INGEGNERIA ELETTRONICA, INFORMATICA ED ELETTRICA

UNIVERSITA' DEGLI STUDI DI PAVIA

DOTTORATO DI RICERCA IN MICROELETTRONICA

AVVISO DI SEMINARIO

Breaking the Speed Limit of a Continuous-Time Delta Sigma ADC by Compensating for More Than One Cycle Excess Loop Delay

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Abstract - The maximum sampling rate of a continuous-time delta sigma modulator in a given process is limited by the minimum flash ADC delay that can be realized. Excess loop delay compensation techniques that are widely used can compensate for delays up to half a clock cycle. Addition of a fast loop outside the flash ADC can break this limit and compensate for upto one and half clock cycles of delay. This technique, along with a low latency flash ADC, and a delay free calibrated DAC, result in a continuous-time delta sigma ADC with the highest reported sampling rate in a 0.18um process. The prototype occupies 0.68mm², consumes 47.6mW,and operates at 800MS/s. In a 16MHz bandwidth(oversampling ratio of 25), the dynamic range, maximum signal to noise ratio, and maximum signal to noise and distortion ratios are 75dB, 67dB, and 65dB respectively. In a 32MHz bandwidth, the dynamic range, maximum signal to noise ratio, and maximum signal to noise and distortion ratios are 64dB,57dB and 57dB respectively.

Biography - Nagendra Krishnapura obtained his BTech from the Indian Institute of Technology, Madras, India and his PhD from Columbia University, New York. He has worked as an analog design engineer at Texas Instruments, Bell Laboratories, Celight Inc., Multilink, and Vitesse semiconductor. He has taught analog circuit design courses at Columbia University as an adjunct faculty. He is currently an associate professor at the Indian Institute of Technology, Madras. His interests are analog and RF circuit design and analog signal processing.

I dottorandi e tutti gli altri interessati sono cordialmente invitati.

L'organizzatore

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