CHAPTER 16
Memory Circuits
Introduction

- The 2 major logic classifications are
  - **Combinational circuits:** Their output depends only on the present value of the input. These circuits do not have memory.
  - **Sequential circuits:** Logic circuits that incorporate memory are called sequential circuits. Their output depends not only on the present value of the input but also on the previous value of the input.

- 2 approaches to provide memory to a digital circuits:
  - **Static sequential circuits:** They employ positive feedback to provide a circuit with 2 stable states (bistable).
  - **Dynamic sequential circuits:** They utilize a capacitor to store the charge.
16.1 Latches and Flip-Flops
16.1.1 The Latch

- The basic memory element, the latch, is shown below.
- Two inverters – Positive feedback
- Bistable circuit with two complementary outputs

Figure 16.1 Basic latch.
16.1.1 The Latch

Figure 16.1 (a) Basic latch. (b) The latch with the feedback loop opened. (c) Determining the operating point(s) of the latch.
Point B is an unstable operating point. By considering the noise that causes positive (negative) small increment at W, the regenerative process will shift the point B upward (downward) to point C (A).

Figure 16.2
16.1.2 The SR Flip-Flop

The latch together with the triggering circuitry forms a flip-flop.

When S/R are raised to 1 simultaneously, Q/\overline{Q} become 0. However, when S/R return to reset state (S=R=0), the state of flip-flop will be undefined.

Figure 16.3 (a) The set/reset (SR) flip-flop and (b) its truth table.
16.1.3 CMOS Implementation of SR Flip-Flops

- The **clocked version** of an SR flip-flop has the 2 cross-coupled inverters as the heart and only NMOS transistors are used in the set-reset circuitry (no conducting path between $V_{DD}$ and ground).

![CMOS implementation of a clocked SR flip flop.](image)

**Figure 16. 4**

- The clock signal is denoted by $\phi$. 

$V_H$ and $V_L$ denote the high and low states of the clock signal, respectively.
The clocked version of an SR flip-flop has the 2 cross-coupled inverters as the heart and only NMOS transistors are used in the set-reset circuitry (no conducting path between $V_{DD}$ and ground).

If the flip-flop stores “0” ($Q=0$ and $\overline{Q}=1$) initially, we wish to set it.

1. Arrange $V_{DD}$ on S input while R is held at 0V.
2. $\phi$ goes high $\Rightarrow$ Q5/Q6 conduct and pull the $V_Q$ down.
3. If $V_Q$ goes below the $V_{TH}$ of Q3/Q4 inverter, it will change state $\Rightarrow V_Q$ rises.
4. The increase of $V_Q$ is fed to Q1/Q2 inverter, causing the $V_{\overline{Q}}$ further down.
The normal operation of the flip-flop is based on 2 important assumptions.

1. Transistors Q5/Q6 supply sufficient current to pull the node $\bar{Q}$ down to a voltage at least slightly below the $V_{TH}$ of Q3/Q4 inverter.
2. The set signal remains high for an interval long enough to cause regeneration to take over the switching process.
16.1.4 A simpler CMOS Implementation of the clocked SR Flip-Flop

Pass-transistor logic is employed to implement the clocked set-reset functions.

Figure 16.7 A simpler CMOS implementation of the clocked SR flip-flop. This circuit is popular as the basic memory cell in the design of static random-access memory (SRAM) chips.
MULTIVIBRATOR CIRCUITS

The flip-flop has two stable states and is called a bistable multivibrator.

There are two other types of multivibrator: monostable and astable.

The monostable multivibrator has one stable state in which it can remain indefinitely. It has another quasi-stable state to which it can be triggered.

Figure 11.9 The monostable multivibrator (one-shot) as a functional block, shown to be triggered by a positive pulse.
A CMOS Monostable Circuit
With Ideal NOR gates
(and Vth=VDD/2)

Figure 11.10  A monostable circuit using CMOS NOR gates. Signal source \( v_I \) supplies positive trigger pulses.
A CMOS Monostable Circuit
With real NOR gates
EFFECT OF: Diodes at each input of a two-input CMOS gate

Figure 11.11  (a) Diodes at each input of a two-input CMOS gate.
(b) Equivalent diode circuit when the two inputs of the gate are joined together. Note that the diodes are intended to protect the device gates from potentially destructive overvoltages due to static charge accumulation.
✓ http://www.doctronics.co.uk/DDE/DDE_04.html#NOR
Figure 11.12 Output equivalent circuit of CMOS gate when the output is (a) low and (b) high.
Figure 11.13 Timing diagram for the monostable circuit in Fig. 11.10.

\[ \tau > (t_{p1} + t_{p2}) \]

\[ \Delta V_1 = \frac{R}{R_{on} + R} V_{DD} \]

Stable state \( V_{o2} = 0 \)

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
Figure 11.13 Timing diagram for the monostable circuit in Fig. 11.10.

Figure 11.14 Circuit that applies during the discharge of C (recovery time) (at the end of the monostable pulse interval T).
For $V_t = V_{DD}/2$ and $R_{on} \ll R$

\[
T = C(R + R_{on}) \ln \left( \frac{R}{R + R_{on}} \frac{V_{DD}}{V_{DD} - V_t} \right)
\]

\[
T = C(R) \ln \left( \frac{R}{R} \frac{V_{DD}}{V_{DD} - \frac{V_{DD}}{2}} \right) = CRLn \left( \frac{2}{-} \right) = 0.69RC
\]
Suppose initially that the trigger input is LOW at a logic level "0" so that the output from the first NOR gate U1 is HIGH at logic level "1", (NOR gate principals). The resistor, $R_T$ is connected to the supply voltage so is also equal to logic level "1", which means that the capacitor, $C_T$ has the same charge on both of its plates. Junction V1 is therefore equal to this voltage so the output from the second NOR gate U2 will be LOW at logic level "0". This then represents the circuits "Stable State" with zero output.

When a positive trigger pulse is applied to the input at time $t_0$, the output of the first NOR gate U1 goes LOW taking with it the left hand plate of capacitor $C_T$ thereby discharging the capacitor. As both plates of the capacitor are now at logic level "0", so too is the input to the second NOR gate, U2 resulting in an output equal to logic level "1". This then represents the circuits second state, the "Unstable State" with an output voltage equal to $+V_{cc}$.

The second NOR gate, U2 will maintain this second unstable state until the timing capacitor now charging up through resistor, $R_T$ reaches the minimum input threshold voltage of U2 (approx. 2.0V) causing it to change state as a logic level "1" value has now appeared on its inputs. This causes the output to be reset to logic "0" which in turn is fed back (feedback loop) to one input of U2. This action automatically returns the monostable back to its original stable state and awaiting a second trigger pulse to restart the timing process once again.

**NOR Gate Monostable Waveforms**
This then gives us an equation for $T$:

$$T = 0.7RC$$

Where, $R$ is in $\Omega$'s and $C$ in Farads.

We can also make monostable pulse generators using special IC's and there are already integrated circuits dedicated to this such as the 74LS121 standard one shot monostable multivibrator or the 74LS123 or the 4538B re-triggerable monostable multivibrator which can produce output pulse widths from as low as 40 nanoseconds up to 28 seconds by using only two external RC timing components with the pulse width given as: $T = 0.69RC$ in seconds.
An Astable Multivibrator Circuit

Figure 11.15  (a) A simple astable multivibrator circuit using CMOS gates.

http://www.doctronics.co.uk/DDE/DDE_03.html#NOT_astables

Animazione senza diodi
An Astable Circuit

Neglecting the finite output resistance of the CMOS gate and assuming that the clamping diodes are ideal (thus have zero voltage drop when conducting).

(b) Waveforms for the astable circuit. The diodes at the gate input are assumed to be ideal and thus to limit the voltage $v_{I1}$ to 0 and $V_{DD}$. 

Microelectronic Circuits - Fifth Edition    Sedra/Smith
An Astable Circuit with ideal diodes

![Diagram of an astable circuit with ideal diodes.](image)
An Astable Circuit with ideal diodes
An Astable Circuit with ideal diodes

Neglecting the finite output resistance of the CMOS gate and assuming that the clamping diodes are ideal (thus have zero voltage drop when conducting).

(b) Waveforms for the astable circuit. The diodes at the gate input are assumed to be ideal and thus to limit the voltage $v_{I1}$ to 0 and $V_{DD}$. 