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Andrea Mazzanti was born in Modena (ITALY) in 1976. He received the *Laurea* and *Ph.D*. degrees in Electrical Engineering from the University of Modena, ITALY in October 2001 and March 2005 respectively.

In 2003 he spent a research period at Agere (Allentown-PA) working on low power CMOS RFICs.

In November 2005 he became assistant professor at the Faculty of Engineering, University of Modena. In January 2010 he joined the Faculty of Engineering of the University of Pavia – ITALY, where he is now Associate Professor. He teaches the courses "Analog IC Design" and "Circuits and Systems for High-speed Communications" to students of the MSc degree in Electronic Engineering.

He started his research activity investigating processing and reliability of III-V transistors for Microwave power applications in collaboration with *Alenia Marconi Systems,* in 2001.

From 2003 his research has been focused to the design of high frequency analog integrated circuits for communications, consumer electronics and medical instruments. The most important contributions are related to building blocks and sub-systems for RF and mmWave transceivers (VCOs, frequency dividers, amplifiers, receiver front-ends and synthesizers).

He participated as principal investigator and co-investigator in several microelectronic research programs, funded by private companies, Italian government and European Community.

At present he is in tight cooperation with *STMicroelectronics* (ST) in the framework of *Studio di Microelettronica*, a research lab joint between University and ST, located inside the Engineering Campus of the University of Pavia. He has also the responsibility of a long-term cooperation agreement with HiSilicon (subsidiary of Huawei), started in 2015, and related to IC design for 5G wireless communications in SiGe BiCMOS technology.

He has been the advisor or co-advisor for more than 30 students in the preparation of their MSc or PhD thesis.

Dr. Mazzanti has published more than 100 papers on international conferences and journals (with 15 the contributions to the IEEE-International Solid State Circuits Conference, ISSCC) which received 1800 citations and the *h* factor is 23 (google scholar). In 2013 he has been included in the *Top Authors* list for the 60 years Anniversary of IEEE ISSCC for having contributed 10 papers in the last 10 years of the conference.

He is IEEE *Senior Member* and serves as reviewer for several journal papers (10 per year, on average) in the area of high frequency integrated circuits.

From 2008 to 2014 he has been member of the TPC of the *IEEE Custom Integrated Circuit Conference* (CICC). Since 2014 he is a member of the TPC of *IEEE International Solid State Circuits Conference* (ISSCC) and the *IEEE European Solid State Circuits Conference* (ESSCIRC).

From 2012 to 2016 he was Associate Editor for the *IEEE Trans. on Circuits and Systems-I* (TCAS-I). He his Guest Editor for the TCAS-I special issue on ISCAS-2016. He has been the Guest Editor for the issues of the *IEEE Journal of Solid State Circuits* dedicated to the 2013 and 2014 editions of IEEE-CICC and 2015 edition of ESSCIRC.

Pavia,

March 2017

Selected Journal Publications

[1] **A.Mazzanti**, P.Uggetti, F.Svelto: *"Analysis and Design of Injection-Locked LC Dividers for Quadrature Generation",* IEEE J. of Solid State Circuits, Vol. 39, no. 9, pp. 1425-1433, Sept. 2004.

[2] **A.Mazzanti**, F.Svelto: *"A 1.8GHz Injection-Locked Quadrature CMOS VCO with Low Phase Noise and High Phase Accuracy"* IEEE Trans. on Circuits and Systems-I: regular papers, Vol. 53, no. 3, pp.554-560, March 2006.

[3] **A.Mazzanti**, L.Larcher, R.Brama, F.Svelto: *"Analysis of Reliability and Power Efficiency in Cascode Class-E PAs",* IEEE J. of Solid State Circuits, Vol.41 no.5, pp.1222-1229, May 2006.

[4] **A.Mazzanti**, F.Svelto, P.Andreani: *"On the Amplitude and Phase Errors of Quadrature LC-Tank CMOS Oscillators",* IEEE J. of Solid State Circuits, Vol.41 no.6, pp.1305-1313, June 2006.

[5] A.Liscidini, **A.Mazzanti**, R.Tonietto: L.Vandi, P.Andreani, R.Castello *"Single-Stage Low-Power Quadrature RF Receiver Front-End: The LMV Cell",* IEEE J. of Solid State Circuits, Vol.41 no.12, pp.2832-2841, Dec. 2006.

[6] G.Cusmai, M.Repossi, G.Albasini, **A.Mazzanti**, F.Svelto: *"A Magnetically Tuned Quadrature Oscillator",* IEEE J. of Solid State Circuits, Vol.42 no.12, pp.2870-2877, Dec. 2007.

[7] R.Brama, L.Larcher, **A.Mazzanti**, F.Svelto: *"A 30.5dBm, 48% PAE CMOS Class-E PA With Integrated Balun for RF Applications",* IEEE J. of Solid State Circuits, Vol.43 no.8, pp.1755-1762, August 2008.

[8] **A.Mazzanti**, E.Sacchi, P.Andreani, F.Svelto *"Analysis and Design of a Double-Quadrature CMOS VCO for Subharmonic Mixing at Ka-Band"* IEEE Trans. on Microwave Theory and Techniques, Vol. 56 no. 2, pp. 355-363, Feb. 2008.

[9] L.Lu, Z.Tang, P.Andreani, **A.Mazzanti**, A.Hajimiri: *"Comments on "Comments on "A General Theory of Phase Noise in Electrical Oscillators"",* IEEE J. of Solid State Circuits, Vol.43 no.9, pp.2170, Sept. 2008.

[10] **A.Mazzanti**, P.Andreani: *"Class C Harmonic CMOS VCOs, with a General Result on Phase Noise",* IEEE J. of Solid State Circuits, Vol.43 no.12, pp.2716-2729, Dec. 2008.

[11] **A.Mazzanti**, P.Andreani *"A Time-Variant Analysis of Fundamental 1/f³ Phase Noise in CMOS Parallel LC-Tank Quadrature Oscillators",* IEEE Trans. on Circuits and Systems I – Regular Papers, Vol.56 no.10, pp. 2173-2180, Oct. 2009.

[12] E.Monaco, M.Pozzoni, F.Svelto, **A.Mazzanti**: "*Injection-locked CMOS Frequency Doublers for* μ*-wave and mm-wave Applications*", IEEE J. of Solid State Circuits, vol.45 no.8, pp. 1567-1574, August 2010.

[13] **A.Mazzanti**, M.Vahidfar, M.Sosio, F.Svelto: "*A Low Phase-Noise Multi-Phase LO Generator for Wideband Demodulators Based on Reconfigurable Sub-Harmonic Mixers*", IEEE J. of Solid State Circuits, vol.45 no. 10, pp.2104-2115, October 2010.

[14] **A.Mazzanti**, M.Sosio, M.Repossi, F.Svelto "*A 24 GHz Subharmonic Direct Conversion Receiver in 65nm CMOS*" IEEE Trans. on Circuits and systems-I: Regular papers, vol.58 no. 1, pp.88-97, January 2011.

[15] F.Vecchi, S.Bozzola, E.Temporiti, D.Guermandi, M.Pozzoni, M.Repossi, M.Cusmai, U.Decanis, **A.Mazzanti**, F.Svelto: "*A Wide-Band Receiver for multi Gbit/s communications in 65nm CMOS*", IEEE J. of Solid State Circuits, Vol.46 no. 3**,** pp.551- 561, March 2011.

[16] U.Decanis, A.Ghilioni, E.Monaco, **A.Mazzanti**, F.Svelto "*A low noise Quadrature VCO based on magnetically coupled resonators and a wide-band frequency divider at mm-waves*", IEEE J. of Solid State Circuits, vol.46 no. 12, December 2012.

[17] **A.Mazzanti**, P.Andreani "*A Push–Pull Class-C CMOS VCO*" IEEE J. of Solid State Circuits, Vol.48 no.3, pp.724-732, March 2013.

[18] A.Ghilioni, **A.Mazzanti**, F.Svelto "Analysis and Design of mm-Wave Frequency Dividers Based on Dynamic Latches With Load Modulation" IEEE J. of Solid State Circuits, Vol.48 no.8, August 2013.

[19] D.Li, Member, G.Minoia, M.Repossi, D.Baldi, E.Temporiti, **A.Mazzanti**, F.Svelto, "A Low-Noise Design Technique for High-Speed CMOS Optical Receivers" IEEE Journal of Solid State Circuits, pp.1437-1447, Vol.49, no.6, June 2014.

[20] E. Mammei, F.Loi, F.Radice, A.Dati, M.Bruccoleri, M.Bassi, **A.Mazzanti**, "Analysis and Design of a Power-Scalable Continuous-Time FIR Equalizer for 10 Gb/s to 25 Gb/s Multi-Mode Fiber EDC in 28 nm LP CMOS" IEEE Journal of Solid State Circuits, pp.3130-3140, Vol.49, no.12, Dec. 2014.

[J20] M. Bassi, F. Radice, M. Bruccoleri, S. Erba, A. Mazzanti "A High-Swing 45 Gb/s Hybrid Voltage and Current-Mode PAM-4 Transmitter in 28 nm CMOS FDSOI" IEEE Journal of Solid State Circuits, pp. 2702 - 2715, Vol.51, no.11, Nov. 2016.

Selected Conference Publications

[1] **A.Mazzanti**, L.Larcher, F.Svelto *"Balanced LC-Tank CMOS Analog Frequency Dividers for Quadrature LO Generation"* Proc. of the IEEE Custom Integrated Circuits Conference (CICC), San Jose (California), Sept. 2005.

[2] A.Liscidini, **A.Mazzanti**, R.Tonietto, L.Vandi, P.Andreani, R.Castello: *"A 5.4mW GPS CMOS Quadrature Front-End Based on a Single-Stage LNA-Mixer-VCO",* IEEE International Solid State Circuit Conference (ISSCC), San Francisco, February 2006.

[3] **A.Mazzanti**, M.Sosio, M.Repossi, F.Svelto: *"A 24GHz Sub-Harmonic Receiver Front-End with Integrated Multi-Phase LO Generation in 65nm CMOS",* IEEE International Solid State Circuit Conference (ISSCC), San Francisco, Feb. 2008.

[4] **A.Mazzanti**, P.Andreani: *"A 1.4mW 4.90-to-5.65GHz Class C CMOS VCO with an Average FoM of 194.5dBc/Hz",* IEEE International Solid State Circuit Conference (ISSCC), San Francisco, Feb. 2008.

[5] **A.Mazzanti**, M.Vahid, M.sosio, F.Svelto: "*A Reconfigurable Demodulator with 3GHz – 5GHz Agile Synthesizer for 9-band WiMedia UWB in 65nm CMOS*", IEEE International Solid State Circuit Conference (ISSCC), San Francisco, Feb. 2009.

[6] E.Monaco, M.Borgarino, F.Svelto, **A.Mazzanti**, *"A 5.2mW Ku-Band CMOS Injection-Locked Frequency Doubler with Differential Input / Output"* Proc. of the IEEE Custom Integrated Circuits Conference (CICC), San Jose (California), Sept. 2009.

[7] S.Bozzola, D.Guermandi, F.Vecchi, M.Repossi, M.Pozzoni, **A.Mazzanti**, F.Svelto, "A Sliding IF Receiver for mm-wave WLANs in 65nm CMOS" Proc. of the IEEE Custom Integrated Circuits Conference (CICC), San Jose (California), Sept. 2009.

[8] **A.Mazzanti**, E.Monaco, M.Pozzoni, F.Svelto: "*A 13.1% Tuning Range 115GHz Frequency Generator Based on an Injection-Locked Frequency Doubler in 65nm CMOS*", IEEE International Solid State Circuit Conference (ISSCC), San Francisco, Feb. 2010.

[9] F.Vecchi, S.Bozzola, M.Pozzoni, D.Guermandi, E.Temporiti, M.Repossi, U.Decanis, **A.Mazzanti**, F.Svelto: "*A wide-band mm-wave CMOS Receiver for Gb/s communications employing inter-stage coupled resonators*", IEEE International Solid State Circuit Conference (ISSCC), San Francisco, Feb. 2010.

[10] A.Ghilioni**,** U.Decanis, E.Monaco, **A.Mazzanti**, F.Svelto, "*A 6.5mW Inductorless CMOS Frequency Divider-by-4 Operating up to 70GHz*", IEEE International Solid State Circuit Conference (ISSCC), San Francisco, Feb. 2011.

[11] U.Decanis, A.Ghilioni, E.Monaco, **A.Mazzanti**, F.Svelto, "*A mm-Wave Quadrature VCO Based on Magnetically Coupled Resonators*", IEEE International Solid State Circuit Conference (ISSCC), San Francisco, Feb. 2011.

[12] D.Bianchi, F.Quaglia, **A.Mazzanti**, F.Svelto: "*A 90Vpp 720MHz GBW Linear Power Amplifier for Ultrasound Imaging Transmitters in BCD6-SOI*", IEEE International Solid State Circuit Conference (ISSCC), San Francisco, Feb. 2012.

[13] A.Ghilioni, E.Monaco, M.Repossi, **A.Mazzanti**: *"A 5mW CMOS wideband mm-wave front-end featuring 17dB of conversion gain and 6.5 dB minimum NF"* in Proc. of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC-2012), pp.447-450, Montreal (Canada), June 2012. ISBN:978-1-4673-0413-9.

[14] D. Li, G. Minoia, M. Repossi, D. Baldi, E. Temporiti, **A.Mazzanti**, F. Svelto: *"A 25Gb/S Low Noise 65nm CMOS Receiver Tailored to 100GBASE-LR4"* in Proc. of the European Solid State Circuits Conference (ESSCIRC), pp. 221-224, Bordeaux (France), September 2012.

[15] A.Ghilioni, U.Decanis, **A.Mazzanti**, F.Svelto: "*A 4.8mW inductorless CMOS Frequency Divider-by-4 with more than 60% Fractional Bandwidth up to 70GHz*" in Proc. of the IEEE Custom Integrated Circuits Conference (CICC), San Jose (California, USA), September 2009.

[16] E.Mammei, E.Monaco, **A.Mazzanti**, F.Svelto: "*A 33.6-to-46.2GHz 32nm CMOS VCO with 177.5dBc/Hz Minimum Noise FOM Using Inductor Splitting for Tuning Extension*" IEEE International Solid State Circuit Conference (ISSCC-2013), Digest of Technical Papers, pp. 350–351, San Francisco (California, USA), February 2013.

[17] F.Radice, M.Bruccoleri, M.Ganzerli, G.Spelgatti, D.Sanzogni, M.Pozzoni, **A.Mazzanti**: "*A 6-bit 6-GS/s 95mW Background Calibrated Flash ADC with Integrating Preamplifiers and Half-Rate Comparators in 32nm LP CMOS*", IEEE European Solid State Circuits Conference (ESSCIRC), pp. 129-132, Sept. 2013.

[18] E.Mammei, F.Loi, F. Radice, A.Dati, M.Bruccoleri, M.Bassi, **A.Mazzanti** "*A Power-Scalable 7-Tap FIR Equalizer with Tunable Active Delay Line for 10-to-25Gb/s Multi-Mode Fiber EDC in 28nm LP-CMOS*", IEEE International Solid State Circuit Conference (ISSCC-2014), Digest of Technical Papers, pp. 142–143, San Francisco (California, USA), February 2014.